



MODEL NO. : G1601FP104GG-001

ISSUED DATE: 2017-12-01

VERSION : A0

- ☒ Preliminary Specification
☐ Final Product Specification

Customer : _____

Approved by	Notes

GVO Confirmed :

Prepared by	Checked by	Approved by
余维	陈礼	陈礼

This technical specification is subjected to change without notice.



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Table of Contents

Table of Contents	3
Record of Revision	4
1 General Specifications	5
2 Input/output Terminals	6
2.1 Main FPC Pin Assignment	6
2.2 Circuit block diagram (Display)	8
2.3 MCU and Display Module Interface Configuration	8
3 Absolute Maximum Ratings	9
3.1 Driving AMOLED Panel	9
4 Electrical Characteristics	9
4.1 Driving AMOLED Panel	9
5 AC Characteristics	10
5.1 MIPI Interface Characteristics	10
5.2 Display RESET Timing Characteristics	12
5.3 TE Timing Characteristics	13
6 Recommended Operating Sequence	14
6.1 Display Power on / off Sequence	14
6.2 Brightness control	15
7 Optical Characteristics Optical Specification	16
8 Environmental / Reliability Test	22
9 Quality Level	23
9.1 AMOLED Module of Characteristic Inspection	23
9.2 Sampling Procedures for each item acceptance table	23
9.3 Inspection Item	23
10 Mechanical Drawing	31
11 Precautions for Use of AMOLED Modules	33
11.1 Handling Precautions:	33
11.2 Storage Precautions:	33
11.3 Transportation Precautions:	33



Record of Revision

[illegible]



1 General Specifications

Feature		Spec	Remark
Display Spec	Screen Size (inch)	6.01	
	Display Mode	AMOLED	
	Resolution(dot)	1080(W)×2160(H)	
	Active Area(mm)	68.256(W)×136.512 (H)	
	Pixel Pitch (um)	63.2 (W)×63.2(H)	
	Technology Type	LTPS	
	Color Depth	16.7M	
	Interface	MIPI 4LANE	
	Surface Treatment	Hard Coating	
Mechanical Characteristics	With TP/Without TP	With TP(on Cell)	
	Module Outline Dimension(W x H x D) (mm)	70.066(W)x140.917(H)x0.723(D)	
	Weight (g)	TBD	
Electronic	Driver IC(Type)	RM69299	
	Touch IC(Type)	GT1151	

Note 1: Requirements on Environmental Protection: RoHS.



2 Input/output Terminals

2.1 Main FPC Pin Assignment

FPC connector: BM24-50DS/2-0.35V(51) (Socket), B-TO-B Connector.

Main board recommended connector: BM24-50DP/2-0.35V(51) (Header), B-TO-B Connector.

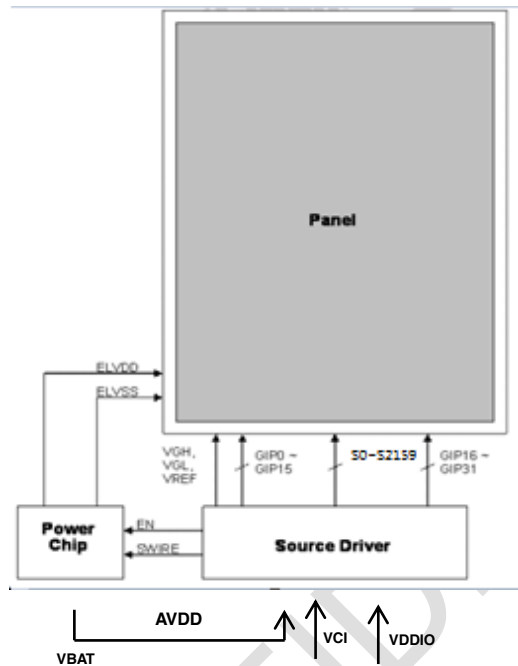
No	Symbol	I/O	Description
1	GND	GND	Ground
2	ELVSS	P	Negative power supply for EL
3	VPP	P	Power supply for MTP Programming or Erase. If it is not used, please let it open.
4	ELVSS	P	Negative power supply for EL
5	GND	GND	Ground
6	ELVSS	P	Negative power supply for EL
7	D3N	I	MIPI data lane
8	GND	GND	Ground
9	D3P	I	MIPI data lane
10	ELVDD	P	Positive power supply for EL
11	GND	GND	Ground
12	ELVDD	P	Positive power supply for EL
13	D0N	I	MIPI data lane
14	ELVDD	P	Positive power supply for EL
15	D0P	I	MIPI data lane
16	GND	GND	Ground
17	GND	GND	Ground
18	RESX	I	Display reset. Active low.
19	CLKN	I	MIPI clock lane
20	AVDD_EN	O	Power IC enable control pin
21	CLKP	I	MIPI clock lane
22	SWIRE	O	Control signal for power IC
23	GND	GND	Ground
24	ERR_FG	O	Error status of MIPI' s HSDT
25	D1N	I	MIPI data lane



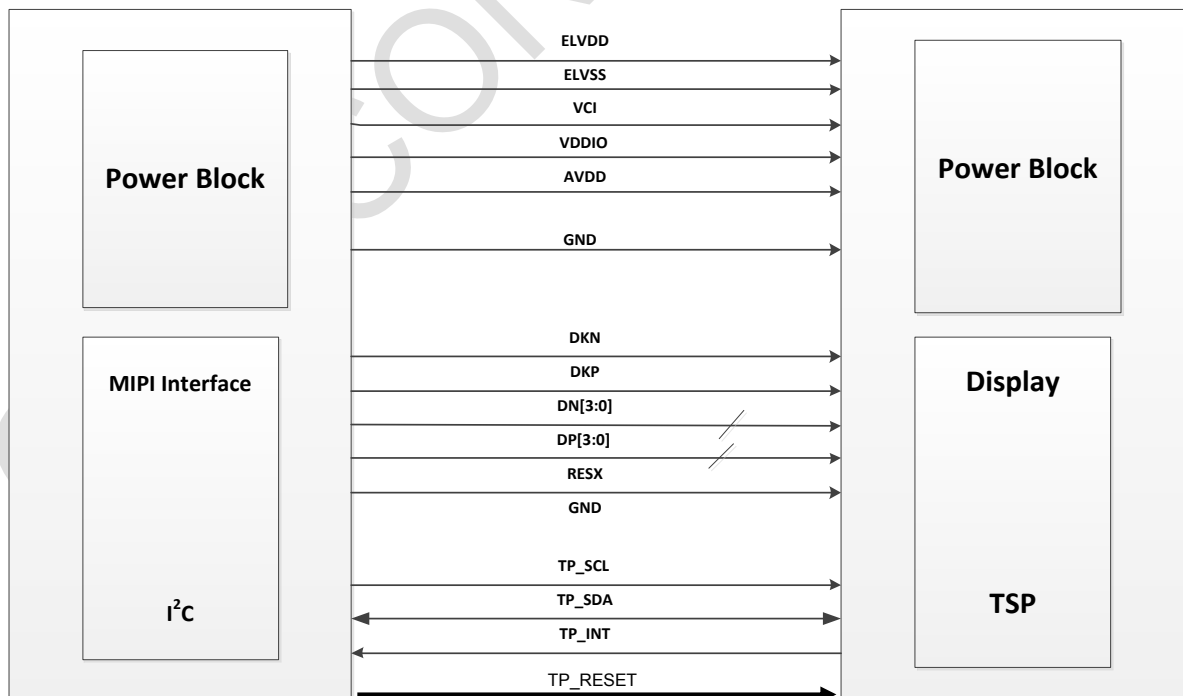
26	PCD	I	panel crack detection
27	D1P	I	MIPI data lane
28	TE	I	Sync Signal for preventing Tearing Effect
29	GND	GND	Ground
30	GND	GND	Ground
31	D2N	I	MIPI data lane
32	TSP_AVDD_3.3V	P	Analog Power for TP
33	D2P	I	MIPI data lane
34	AVDD	P	Power supply for Analog system
35	GND	GND	Ground
36	VCI	P	Power supply for display analog circuits
37	TSP_DVDD_1.8V	P	Power supply for TP logic circuits
38	VDDIO	P	Power supply for interface system except MIPI/MDDI interface
39	TSP_TA	NC	
40	GND	GND	Ground
41	TSP_INT	I	Interrupt signal for TP
42	F_SCLK	I	Flash signal
43	TSP_SCL	I	SCL pin for TP
44	F_CSN	I	Flash signal
45	TSP_SDA	I/O	SDA pin for TP
46	F_IO<0>	I/O	Flash signal
47	TSP_RESET	I	Reset Pin for TP, Active low.
48	F_IO<1>	I/O	Flash signal
49	GND	GND	Ground
50	GND	GND	Ground

Note: I=Input; O=Output; P=Power; I/O=Input / Output

2.2 Circuit block diagram (Display)



2.3 MCU and Display Module Interface Configuration





3 Absolute Maximum Ratings

3.1 Driving AMOLED Panel

Maximum Ratings (Voltage Referenced to VSS) Vss=0V, Ta=25°C

Item	Symbol	MIN	MAX	Unit
Analog Power supply	VCI	-0.3	+5.5	V
Logic Power supply	VDDIO	-0.3	+5.5	V
Positive Power Input	ELVDD	-	+5.0	V
Negative Power Input	ELVSS	-5.0	-	V
TP power supply Input	TSP_AVDD	-0.3	+4.2	V
TP power supply for logic circuits	TSP_DVDD	-0.3	+4.2	V

Note: Functional operation should satisfy the limits in the Electrical Characteristics tables or Pin Description section. If the module exceeds the absolute maximum ratings, permanent damage may occur. Besides, if the module is operated with the absolute maximum ratings for a long time, the reliability may also drop.

4 Electrical Characteristics

4.1 Driving AMOLED Panel

Item		Symbol	MIN	TYP	MAX	Unit
Logic Power supply		VDDIO	1.65	1.80	3.3	V
Analog Power supply		VCI	2.5	2.80	3.60	V
ELVDD Supply Voltage		ELVDD	4.55	4.60	4.65	V
ELVSS Supply Voltage		ELVSS	-5	-3	-	V
TP power supply Input		TSP_AVDD	2.6	2.8	3.3	V
TP power supply for logic circuits		TSP_DVDD	1.53	1.8	3.3	V
Input Signal Voltage	High Level	VIH	0.80*VDDIO	-	VDDIO	V
	Low Level	VIL	0.00	-	0.20*VDDIO	V
Output Signal Voltage	High Level	VOH	0.80*VDDIO	-	VDDIO	V
	Low Level	VOL	0.00	-	0.20*VDDIO	V
Normal		I _{ELVDD} / I _{ELVSS}	-	TBD	TBD	mA
		I _{VCI}	-	TBD	TBD	mA
		I _{VDDIO}	-	TBD	TBD	mA
		I _{avdd}	-	TBD	TBD	mA
Stand-by		I _{VCI}	-	TBD	TBD	uA
		I _{VDDIO}	-	TBD	TBD	uA

Ta=25°C



Note1: The input digital voltage is the I/O reference voltage.

Note2: VDDIO usually ranges from 1.65V to 3.3 V. If VDDIO is changed, the remaining voltage needs to be changed to the same voltage as VDDIO.

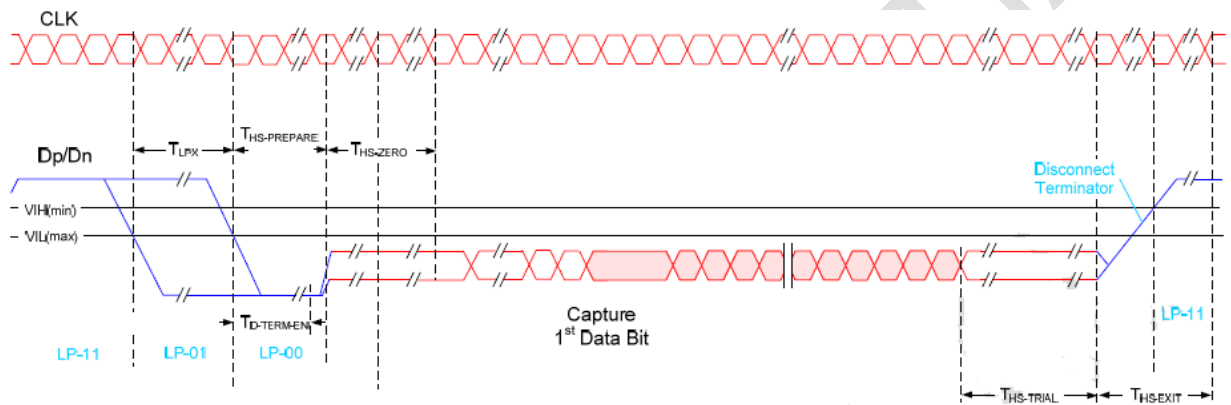
Note3: Under full white pattern, Video Mode 60Hz.

Note4: 60Hz command mode at 800 Mbps.

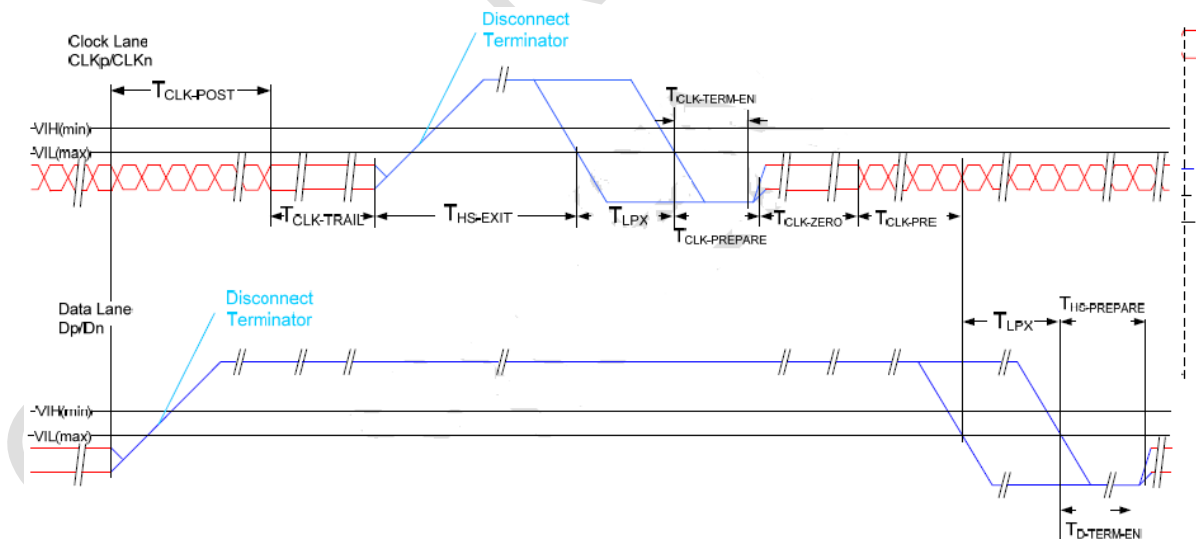
5 AC Characteristics

5.1 MIPI Interface Characteristics

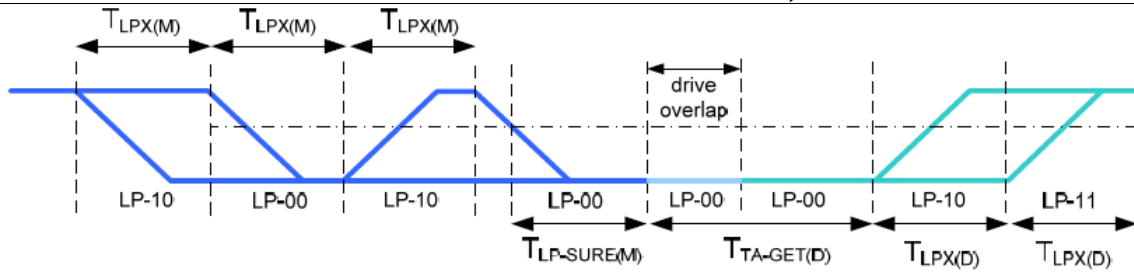
HS Data Transmission Burst



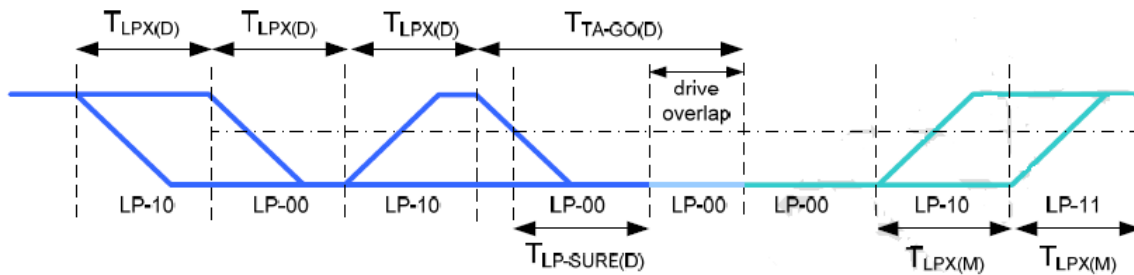
HS clock transmission



Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	$60ns + 52*UI$			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		$35 ns + 4*UI$	

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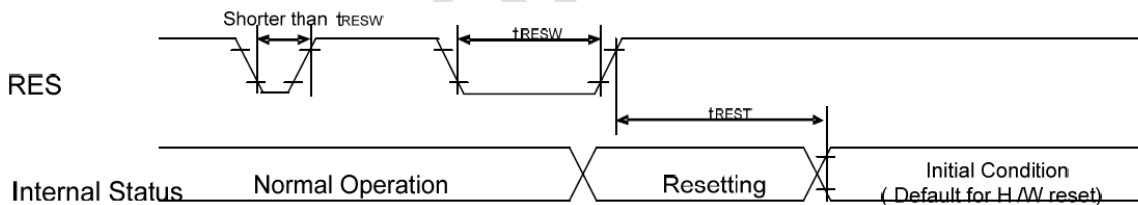


$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	$40ns + 4*UI$		$85 ns + 6*UI$	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145ns + 10*UI$			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$60ns + 4*UI$			ns

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

5.2 Display RESET Timing Characteristics

Reset input timing:



VDDIO=1.65 to 3.3V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85°C

Timing Parameters

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Note1. Spike caused by an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

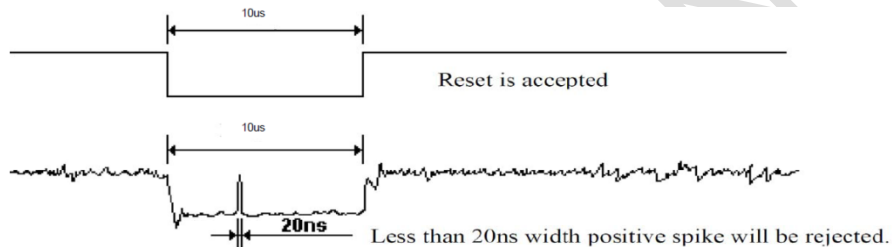
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RESX Pulse	Action
Shorter than 5 μ s	Reset Rejected
Longer than 10 μ s	Reset
Between 5 μ s and 10 μ s	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blank (The display is entering blanking sequence, whose maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains blank in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

5.3 TE Timing Characteristics

Mode1, The Tearing Effect Output line consists of V-Blanking information only.



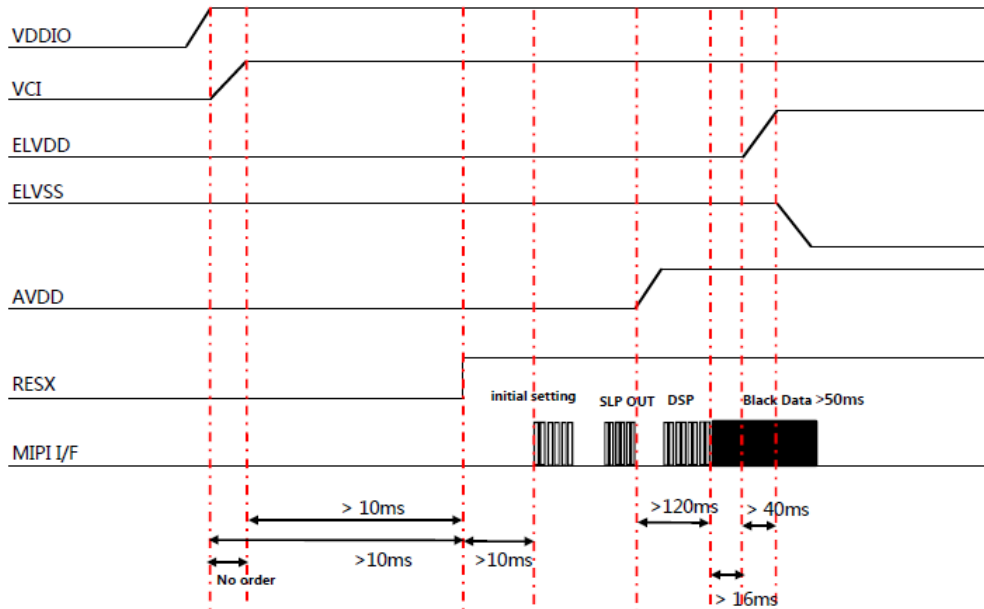
Tvdh = The display is not updated from the frame memory.

Tvdl = The display is updated from the frame memory.

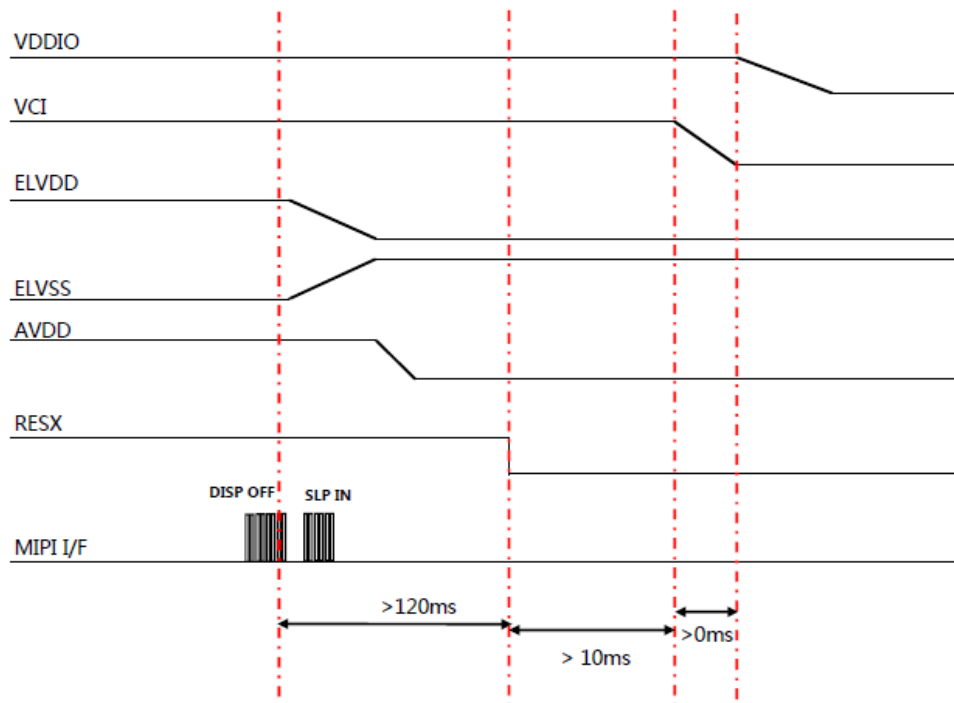
6 Recommended Operating Sequence

6.1 Display Power on / off Sequence

6.1.1 Power On Sequence



6.1.2 Power Off Sequence





6.2 Brightness control

Use “command 5100h, data xxh” to adjust the Manual Brightness value of the display:

In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

Inst/Para	R/W	Address		Date Type	Description
		MIPI	Other		
BRTCTRL	W	51h	5100h	Hex	Value form 0~255(FF)



7 Optical Characteristics Optical Specification

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angle		θT	CR≥10	80	-		Degree	Note 2 Test Equipment: CS2000A
		θB		80	-			
		θL		80	-			
		θR		80	-			
Contrast Ratio		CR	θ=0°	100000				Note1,Note3 Test Equipment: CS2000A
Response Time		T _{ON}	25℃			1	ms	Note1,Note4 Test Equipment: Admesy MSE
		T _{OFF}						
Chromaticity	White	x		(0.280)	(0.300)	(0.320)		Test Equipment: CS2000A Note: Chromaticity can be modified according to customer demand
		y		(0.295)	(0.315)	(0.335)		
	Red	x		(0.625)	(0.655)	(0.685)		
		y		(0.315)	(0.345)	(0.375)		
	Green	x		(0.210)	(0.250)	(0.290)		
		y		(0.670)	(0.710)	(0.750)		
	Blue	x		(0.105)	(0.135)	(0.165)		
		y		(0.030)	(0.060)	(0.090)		
Uniformity		U		75			%	Note1,Note6 Test Equipment: CS2000A
NTSC				90	100		%	Note5
Luminance		L	Normal	365	430	495	Cd/m ²	Note1,Note7 Test Equipment: CS2000A
Cross-talk						1.5	%	Note8 Test Equipment: CS2000A
Gamma				2.0	2.2	2.4		Gamma=2.2±0.2 Test Equipment: CS2000A

Test Conditions:

the ambient temperature is 25°C.

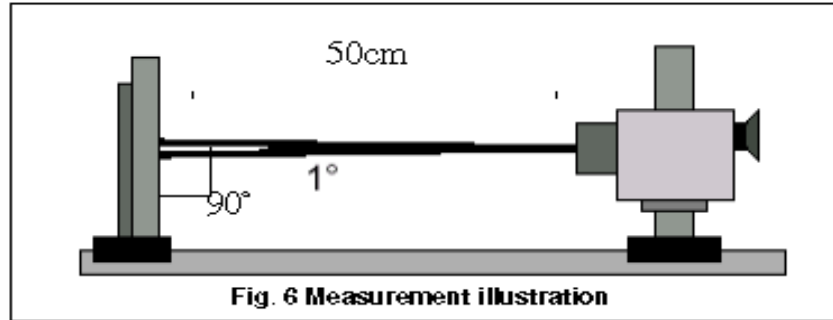


1. The test systems refer to Note1 and Note2.

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Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the AMOLED screen. All input terminals AMOLED panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

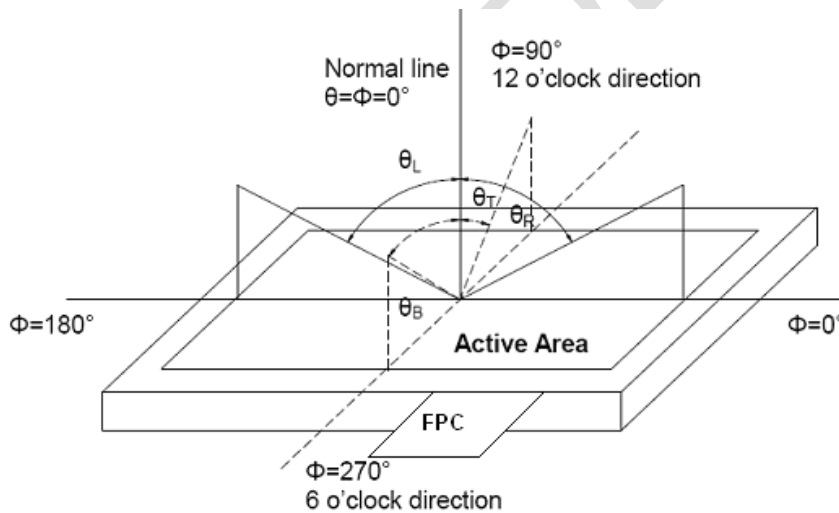


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

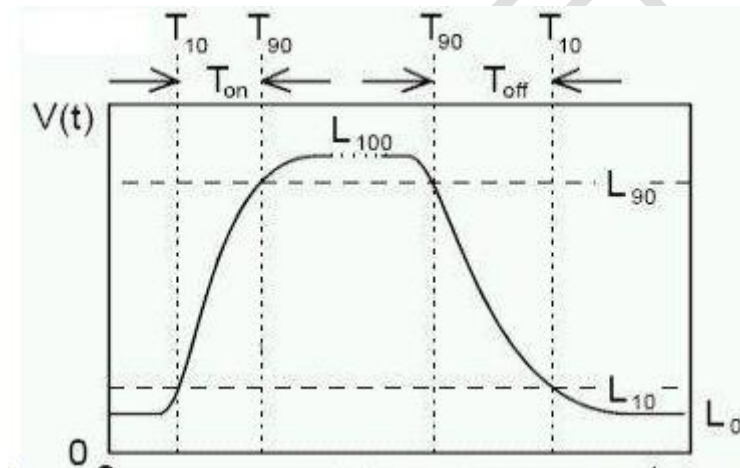
$$\text{Contrast ratio(CR)} = \frac{\text{Luminance measured when LCD is on the "white" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

“White state “: A state where the AMOLED should be driven by Vwhite.

“Black state”: A state where the AMOLED should be driven by Vblack.

Note 4: Definition of response time

The response time is defined as the AMOLED optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changing from 10% to 90%. And fall time (T_{OFF}) is the time between photo detector output intensity changing from 90% to 10%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates are measured at the center point of AMOLED.

Note 6: Definition of luminance uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity}(U) = L_{\min} / L_{\max}$$

L-----Active area length W----- Active area width

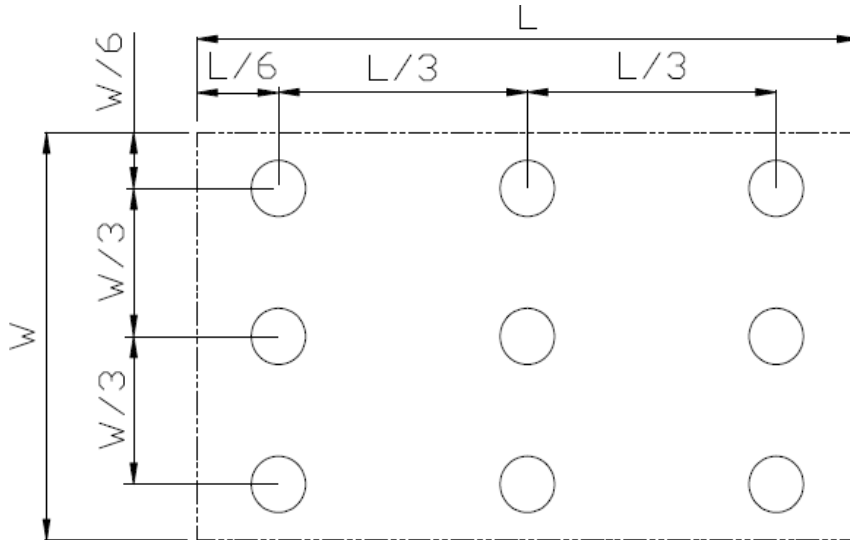


Fig. 2 Definition of uniformity

L_{\max} : The measured maximum luminance of all measurement position.

L_{\min} : The measured minimum luminance of all measurement position.

Note 7: Definition of luminance:

Measure the luminance of white state at the center point.

Note 8: Cross Talk

A. Measure luminance at the position, P0.

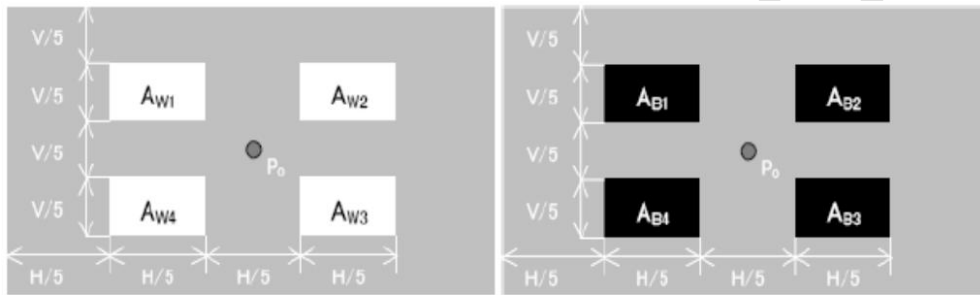
B. Calculate cross talk as below equation.

$$L_{W_OFF} = \frac{L_{W1} + L_{W2} + L_{W3} + L_{W4}}{4}$$

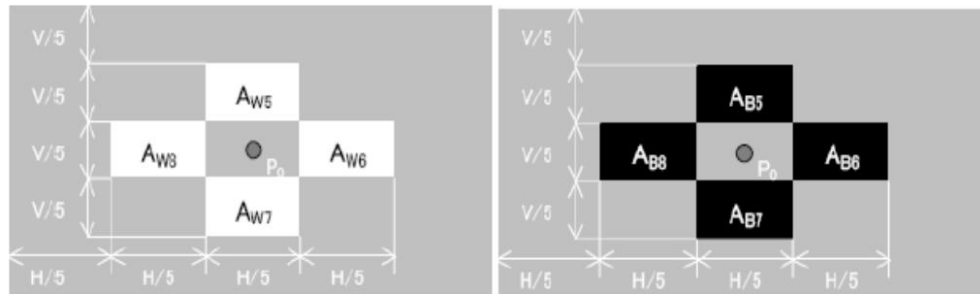
$$L_{B_OFF} = \frac{L_{B1} + L_{B2} + L_{B3} + L_{B4}}{4}$$

$$\text{crosstalk} = \frac{|L_{Wi_ON} - L_{W_OFF}|}{L_{W_OFF}} \times 100\% \quad (i = 5 \text{ to } 8)$$

$$\text{crosstalk} = \frac{|L_{Bi_ON} - L_{B_OFF}|}{L_{B_OFF}} \times 100\% \quad (i = 5 \text{ to } 8)$$

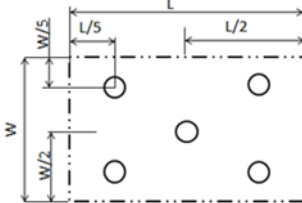


(a) L_{W_OFF} , L_{B_OFF} measuring pattern



(b) L_{W_ON} , L_{B_ON} measuring pattern

8 Environmental / Reliability Test

No	Test Item	Condition	Remark
1	High Temperature Operation	+70℃, 120hrs	According to the customer request
2	Low Temperature Operation	-20℃, 120hrs	According to the customer request
3	High Temperature Storage	+80℃, 120hrs	According to the customer request
4	Low Temperature Storage	-30℃, 120hrs	According to the customer request
5	High Temperature & High Humidity Operation	60℃, 90% RH, 120hrs	According to the customer request
6	High Temperature & High Humidity Storage	60℃, 90% RH, 120hrs	According to the customer request
7	Thermal Shock (Non-operation)	-30℃ (30 min) ~ +70℃ (30 min), Change time: 10min, 30Cycles	According to the customer request
8	Electro Static Discharge (Operation)	<p>C=150pF, R=330Ω, 5points/panel Air: ±8KV, 5times; Contact: ±4KV, 5 times; (Environment: 15℃~35℃, 30%~60%, 86Kpa~106Kpa).</p> 	IEC61000-4-2 GB/T17626.2



9 Quality Level

9.1 AMOLED Module of Characteristic Inspection

The environmental condition and visual inspection shall be conducted as below:

- (1) Ambient temperature: $23 \pm 3^{\circ}\text{C}$
- (2) Humidity: $55 \pm 10\%\text{RH}$
- (3) Ambient light intensity of visual inspection: 800 ~ 1200 lux
- (4) Ambient light intensity of function inspection: $\leq 200\text{lux}$
- (5) Viewing Distance: $30 \pm 5\text{cm}$
- (6) Viewing angle (tolerance): the front side 45° (Z) $\pm 15^{\circ}$
- (7) Inspection time: $10 \pm 5\text{ sec}$

9.2 Sampling Procedures for each item acceptance table

Defect type	Sampling Procedures	AQL
Major defect	GB/T2828.1-2003 Inspection level II normal inspection single sample inspection	0.65
Minor defect	GB/T2828.1-2003 Inspection level II normal inspection single sample inspection	1.0

Major defect:

Any defect may result in functional failure, or reduce the usability of product for its purpose. For example, electrical failure, deformation and etc.

Minor defect

A defect does not reduce the usability of product for its intended purpose and un-uniformity, such as dot defect and etc.

The criteria on major and/or minor judgment will be according with the classification of defects.

9.3 Inspection Item

No	Item	Area	Criterion of Defect			Defect type
			Type	DS	Acceptable number	
1	Dot Defect	AA	Bright Dot	$\geq 10\text{mm}$	0	Minor
			Dark Dot	$\geq 10\text{mm}$	4	
			Dark Dot (≥ 2)	$\geq 10\text{mm}$	2	

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			connections)				
2	No Display	AA	/			Not allowed	Fatal
3	Abnormal Display	AA	/			Not allowed	Fatal
4	Normally white	AA	/			Not allowed	Fatal
5	Line Defect	AA	single line	Bright line	Not allowed	Fatal	
				Dark line	Not allowed		
			Multiple lines	Bright line	Not allowed		
				Dark line	Not allowed		
			Half-Line	Bright line	Not allowed		
				Dark line	Not allowed		
6	Image sticking	AA	Switch to the next screen and display the image of the previous picture				Major
7	Color & Edge Mura	AA	See limit sample(under full white screen)				Major
8	Color crast	AA	See limit sample(under full white screen)				Major
9	Water Ripple	AA	Not allowed				Major
10	Other mura(Low gray-scale white spot、S-Line Mura)	AA	Not allowed(under full white screen) or See limit sample(under low gray-scale white screen)				Major
11	TP	AA	TP function NG			Not allowed	Fatal
12	Glass crack	AA、OA	/			Not allowed	Fatal
13	Screen bump	AA、OA	Encap surface is not allowed and LTPS does not affect assembly				Major
14	Line sefects (light visible)	AA	W (mm)	L (mm)	DS (mm)	Acceptabl e number	Minor
			W≤0.03	-	-	Ignore	
			0.03<W≤0.05	L≤5.0	≥10	2	
			0.05<W	-	-	0	
			-	L>5.0	-	0	
15	Point sefects (light visible)	AA	D (mm)	DS (mm)		Acceptabl e number	Minor
			D≤0.1	/		Ignore	



			0. 1<D≤0. 25	≥10		2	
			0. 25<D	-		0	
16	Glass scratch	AA	W（mm）	L（mm）	DS（mm）	Acceptabl e number	Minor
			W≤0.03	L<5.0	≥10	Ignore	
			0.03<W≤0.05	L≤2.0	≥10	Ignore	
				2.0<L≤5.0	≥10	2	
			0.05<W	-	0	0	
				L>5.0	0	0	
17	Frit Encapsulation	FA	Frit width uniformity. It should not have bubble or breakage.				Major
18	Polarizer crease / indentation	AA	See limit sample				Minor
19	Protective film starved/overflow glue/burr	Except AA	No control under W≤0.3mm				Minor
20	Polarizer bump point	Whole area	Bump:D≤0.25mm, dent ≤1mm or See limit sample		Allow 3		Minor
21	Polarizer bubble line	Out of AA, ≤0.25m m	Encap surface		Not allowed		Minor
22	Scratches on the surface of polarizer	Whole area	No harm subject regardless of control				Minor
23	Concave dot、Black and white dot、Polarizer Dent/Bubble	AA	Front（Encap surface）	D（mm）	DS（mm）	Acceptabl e number	Minor
				D≤0.1	≥10	Ignore	
				0.1<D≤0.2	≥10	3	
				0.2<D	≥10	0	
			Metal material foreign material	/	≥10	Not allowed	
24	Polarizer Scratch/Fiber(Linear)	AA	W（mm）	L（mm）	DS（mm）	Acceptabl e number	Minor
			W≤0.03	L≤5.0	≥10	Ignore	
			0.03<W≤0.05	L≤2.0	≥10	Ignore	
				2.0<	≥10	3	



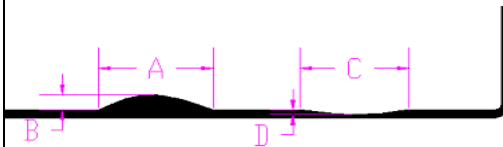

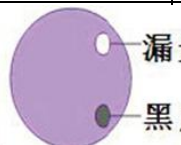
			0.05<W		-	≥10	0	
					L>5.0	≥10	0	
25	Edge/Side breakage	OA	The following Criterion is applicable to any side (unit: mm)					Minor
			Z	X	Y	Acceptable number		
			≤ T	≤2.0	not extended to circuit Area or Frit	<5		
26	UV glue	Not IC side	Over coating				Not allowed	Minor
		IC side	The coating of IC side is not higher than POL.				Not allowed	
		IC side	The coating of IC side is not higher than POL.				Not allowed	
27	Tuffy glue	IC and FPC bonding area	The coating should not have breakage or Bubble.					Minor
			The coating is not higher than POL.					
		Other area	Tuffy glue is not allowed to interrupt and the diameter of Bubble is not more than 0.5mm.					
			The coating is not higher than POL.					
		IC	Not allowed					
		FPC	Ribbon glue: the width is not more than 1mm. Dot glue: the diameter is not more than 2mm.					
28	Rear reinforcement glue of FPC	FPC	The width is not more than 1mm . The height is lower than LTPS.					Minor
29	ACF	Bonding Area	The length of attachment is more than both ends of FPC, which should be range from 0.2 to 1mm. Don't go beyond the edge of panel. Effective lap width of wiring ACF is more than 2/3, which is compared with the width of the gold finger of FPC. Don't have bubble or wrinkle.					Minor
30	FPCA	FPC	The component can not reverse polarity					Minor
			No wrong insertion					
			FPC should not have serious crease which destroy the line, prick and spots damage. Scratch is not allowed if Cu layer is exposed.					
			The gold fingers should not be oxidized, scraped, folded, impressed, broken, spotted or dissymmetry.					
			Make sure FPC is not scalded, with its location holes not having deficiency or obviously shift.					
			The component of FPC should be the same as BOM					

			list.	
			No remaining soldering Sn	
			No visual particle on the pad line	
31	FPC bonding	Bonding area	Bubble: Visible bubble is not allowed	Minor
	FPC Skew		Overhang : The size above 1/2 of soldering electrode of the parts overhang to the LAND is prohibited. The tilt height less than 0.5mm between FPC and foam.	
			Not allowed	
32	Package	Other	Products should put into the anti-static trays, with non-overlapping, and the trays should be staggered placed.	Minor
			Different products cannot be mixed into the same inner package.	
			The package should not have obvious deformation or breakage .The printing labels type and quantity are correct.	
			The package should have QC signature. ROHS label is needed if the product is under ROHS control.	

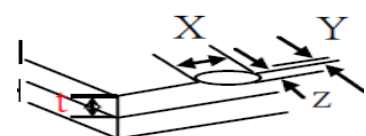
Inspection standard for cover

No	Item	Area	Criterion of Defect				Defect type
33	Cover dot、Black and white dot、Polarizer Dent/Bubble	Whole area	D (mm)	DS (mm)	Acceptable number		Minor
			$D \leq 0.15\text{mm}$	/	Ignore (specks is not allowed)		
			$0.15\text{mm} < D < 0.25\text{mm}$	$DS \geq 10\text{mm}$	2		
			$D > 0.25\text{mm}$	/	Not allowed		
			Specks: $D < 0.15\text{mm}$, $N > 5$ in $10\text{mm} \times 10\text{mm}$ area				
34	Cover Scratch/ Fiber(Linear)	AA	W(mm)	L(mm)	DS(mm)	Acceptable number	Minor
			$W \leq 0.03\text{mm}$	$L \leq 10\text{mm}$	≥ 10	Ignore	
			$0.03\text{mm} < W \leq 0.05\text{mm}$	$L \leq 5.0\text{mm}$	≥ 10	2	
			$W > 0.05$	/	/	Not allowed	
			/	$L > 5.0\text{mm}$	/	Not allowed	
			Not allowed to scratch				
35	Edge pinhole	Edge of cover	D (mm)	DS (mm)	Acceptable number		Minor
			$D < 0.1\text{mm}$	$DS \geq 10\text{mm}$	one is allowed on each side		

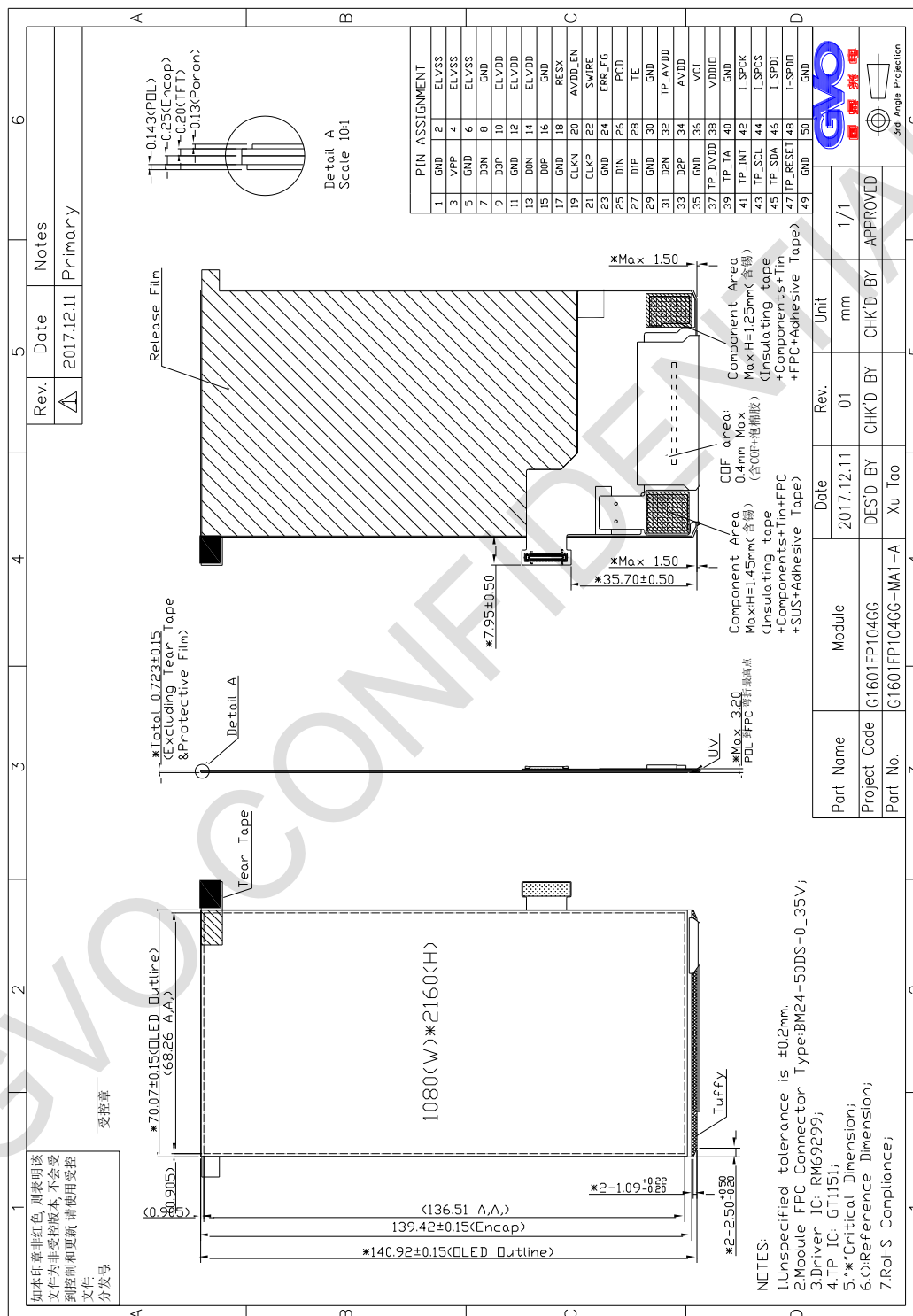


36	Uneven edge of the ink	Edge of cover	W (B or D)	L(A or C)	Acceptable number	Minor	
			$W\leq 0.15\text{mm}$	$L\leq 3\text{mm}$	≤ 2		
							
37	ink silk screen serrated	OA area	D (mm)	DS (mm)	Acceptable number	Minor	
			$D\leq 0.2$	$DS\geq 10\text{mm}$	2		
38	Camera Hole	OA area	breakage or crack: $D\leq 0.1\text{mm}$			Minor	
			Hole is not round: Refer to the limit sample				
			Dot Defect: $D\leq 0.1\text{mm}$, and $N\leq 1$, heterochrosis and line defect are not allowed;				
			Camera hole smudge: not allowed				
39	Printing defect	OA area	Wrongly、Missing、Ghosting and incomplete printing : not allowed			Minor	
			Fonts consistent with the standard characters, no significant difference in visualization				
			Penetrating scratch is not allowed				
40	IR Hole/ Black spots/ Line scratch foreign matter/ Residue	OA area	DS(mm)	Acceptable number			Minor
			$DS<0.1$	Ignore			
			$0.1\leq DS\leq 0.15$	1			
			Note: Not visible on black background, don't affect the transmission rate				
			Foreign body, dirty in IR hole: not allowed				
			Scratched\Line defects in IR hole: $W\leq 0.03\text{mm}$, $L\leq 1\text{mm}$, $N\leq 1$, Not visible on black background, don't affect the transmission rate.				
			Residual glue in IR hole: not allowed				
41	Cover lens deformation	OA area	Raised height $<0.15\text{mm}$, and the area is less than 25% of the entire non-display area in the cover lens			Minor	
		AA area	Deformation is not allowed in AA area				

42	Poor penetration of icons	OA area	DS≤0.15 and N≤1		Minor
43	Cover dirt	Whole area	Not allowed		Minor
44	Cover crack				Fatal flaw
45	Cover paint chips				
46	Burr	Edge of cover	L≤0.05mm, W<0.2mm accept (The premise does not affect the assembly and function and user operation)		Minor
47	colour difference	OA area	No significant difference in visualization (refer to the limit sample if necessary)		
48	Overfill	Whole area	Not allowed in AA area		Minor
			The visible part of the periphery can not be seen after assembly, and can not affect the assembly		
49	Protective film	Whole area	Film position deviation≤0.15mm		Minor
			Scratch: no control when don't damage the body		
			Overfill/ lack of plastic/ Burr: no control		
			Not control the bubble inside the cover protection film		
50	Easy to tear	Cover surface	Function failure\ damaged\ Missing label: not allowed		
			Wrinkle\ Convex-concave point\dirty\ punching\burr\ squeeze out: not control		
51	Composite tape	LTPS	Don't go beyond the edge of panel.		
			Folds\ Light leakage\ Impact assembly or thickness: not allowed		
			Damaged: not allowed		
			Bump does not affect the assembly: not control		
			Punching the bad size meet the drawings requirements: not control		
			Non-wipe dirty\foreign body: not allowed Foreign objects in accordance with the standard line/point		
			Burr does not exceed the screen edge: not control		
			Do not have obvious bubbles Gumflower\Overfill: no control		
52	Film warpage	Whole area	Warpage ≤0.2mm		Minor
53	ICON hole	OA area	chromatic aberration、double image、dot defect 、line defect: not allowed (or refer to limited sample)		Minor
54	Earpiece hole	OA area	left-right asymmetry , Hole Rather large/small or off normal(Out of specification)No chamfer, Uneven polishing: not allowed		
55	Ink bumps	OA area	Positive side reference point defects; The back side does not affect the assembly; Ink overflow or		

			accumulation: not allowed					
56	Cover concave convex point	Whole area	Front : Height & depth ≤ 0.15mm, size ≤ 0.4mm, if necessary reference limit sample					
			Back: Don't affect the fit process is not controlled					
57	Insulation Tape	Bonding area	Obvious wrinkles and bubbles: not allowed				Minor	
		Component area	Scratch/ Gumflower: not control					
			Non-wipe dirty: not allowed					
			Offset can not exceed the edge of the product, Others are required to the drawings					
			Burr\ Overfill: not control					
			Damaged/incomplete/missing paste: not allowed					
58	Cover edge/side breakage	Edge of cover	X	Y	Z	DS	Acceptable number	Minor
			X<0.2mm	Y<0.2mm	Z≤1/2t	DS > 5mm	Unilateral ≤2	
			X>0.2mm	/	/	not allowed		
			/	Y>0.2mm	/	not allowed		
			/	/	Z>1/2T	not allowed		
			Cracks are not allowed					
59	Blunt	Whole area	Not allowed				Fatal flaw	
60	Fit bubble	AA	According to the punctate specifications				Minor	
61	Vision area edge defect	OA	D≤0.2mm, DS>10,N≤2 (hole saw tusk less than 2) , if necessary reference limit sample.				Minor	
62	Cover heterochrosis	OA	Heterochrosis side execute according to point defect size, bulk/stick refer to Limited sample				Minor	

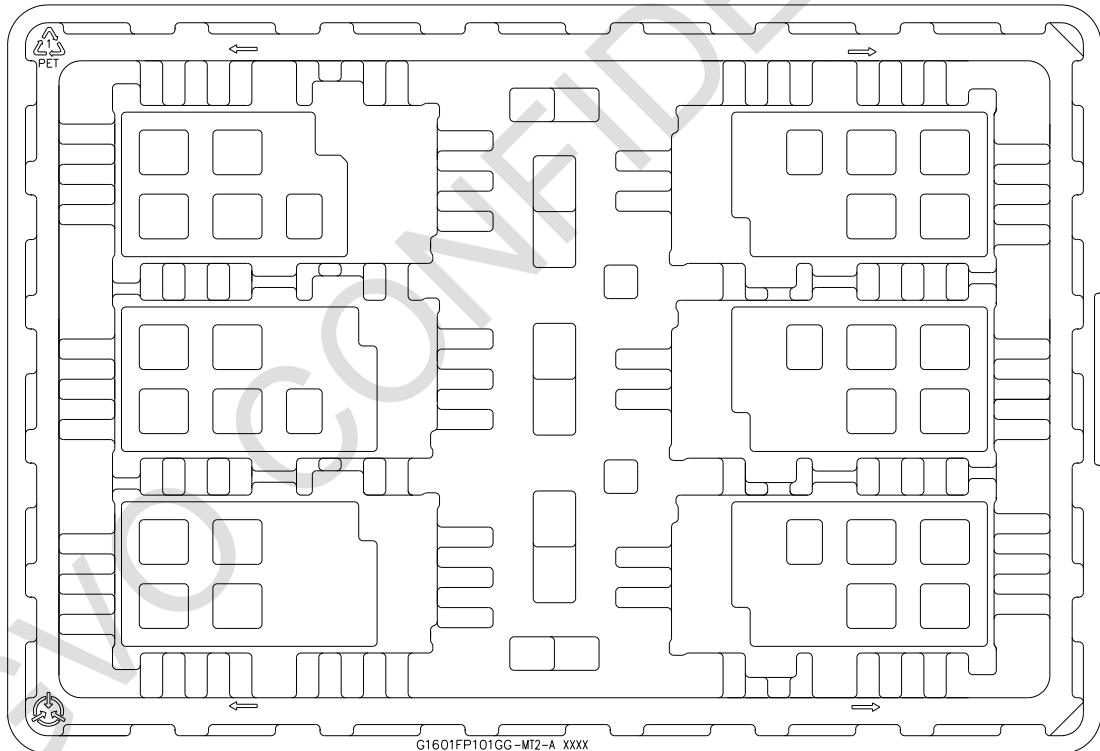
10 Mechanical Drawing



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Packing Drawing

Packing Condition	Contents
Packing Type	TRAY + Carton packing type
TRAY material model	tray ($10^5 \sim 10^9 \Omega$)
Tray packing type	See the picture 1
Number of panels per tray	6 pieces
Number of Tray per carton	28units ((26 units + 2empty)PET tray)
Number of panels per carton	156pieces



Picture 1



11 Precautions for Use of AMOLED Modules

11.1 Handling Precautions:

- 11.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from height.
- 11.1.2 Do not press down the screen on the adjoining areas too hard because the color tone may be shifted.
- 11.1.3 The polarizer covering the display surface of the AMOLED module is soft and easily scratched. Handle this polarizer carefully.
- 11.1.4 If the display surface is contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is still not completely clear, moisten the cloth with ethyl alcohol.
- 11.1.5 Solvents may damage the polarizer. Do not use water, ketone or aromatic solvents except ethyl alcohol.
Do not attempt to disassemble the AMOLED Module.
- 11.1.6 If the logic circuit power is off, do not apply the input signals.
- 11.1.7 To prevent destruction from static electricity, be careful to maintain an optimum working environment.
- 11.1.8 Be sure to make yourself in contact with the ground when handling with the AMOLED Modules.
- 11.1.9 Tools required for assembly, such as soldering irons, must be properly ground.
- 11.1.10 To reduce the generation of static electricity, do not conduct assembly or other work under dry conditions.
- 11.1.11 To protect the display surface, the AMOLED Module is coated with a film. Be careful when peeling off this protective film, because static electricity may generate.

11.2 Storage Precautions:

- 11.2.1 When storing the AMOLED modules, be sure that they are not directly exposed to the sunlight or the light of fluorescent lamps.
- 11.2.2 The AMOLED modules should be stored under the storage temperature range. If the AMOLED modules will be stored for a long time, the recommended condition is:
Temperature: 0°C~40°C Relatively humidity: ≤80%
- 11.2.3 The AMOLED modules should be stored in the room without acid, alkali or harmful gas.

11.3 Transportation Precautions:

- 11.3.1 The AMOLED modules should not be suffered from falling and violent shocking during transportation. Besides, excessive press, water, damp and sunshine, should be avoided.