億都集團
YEEBO GROUP

SPECIFICATION
FOR
LCD MODULE

MODULE NO: YB-TG320480S07A-C-C0

Doc.Version:00

Customer Approval:

☐ Accept	☐ Reject

YEEBO	NAME	SIGNATURE	DATE
Prepare	Electronic Engineer	李林	2019-2-17
Check	Mechanical Engineer	陳長吉	2019-2-18
Verify			
Approval		崔化	2019-02-18

☐APPROVAL FOR SPECIFICATIONS ONLY

■APPROVAL FOR SPECIFICATIONS AND SAMPLE

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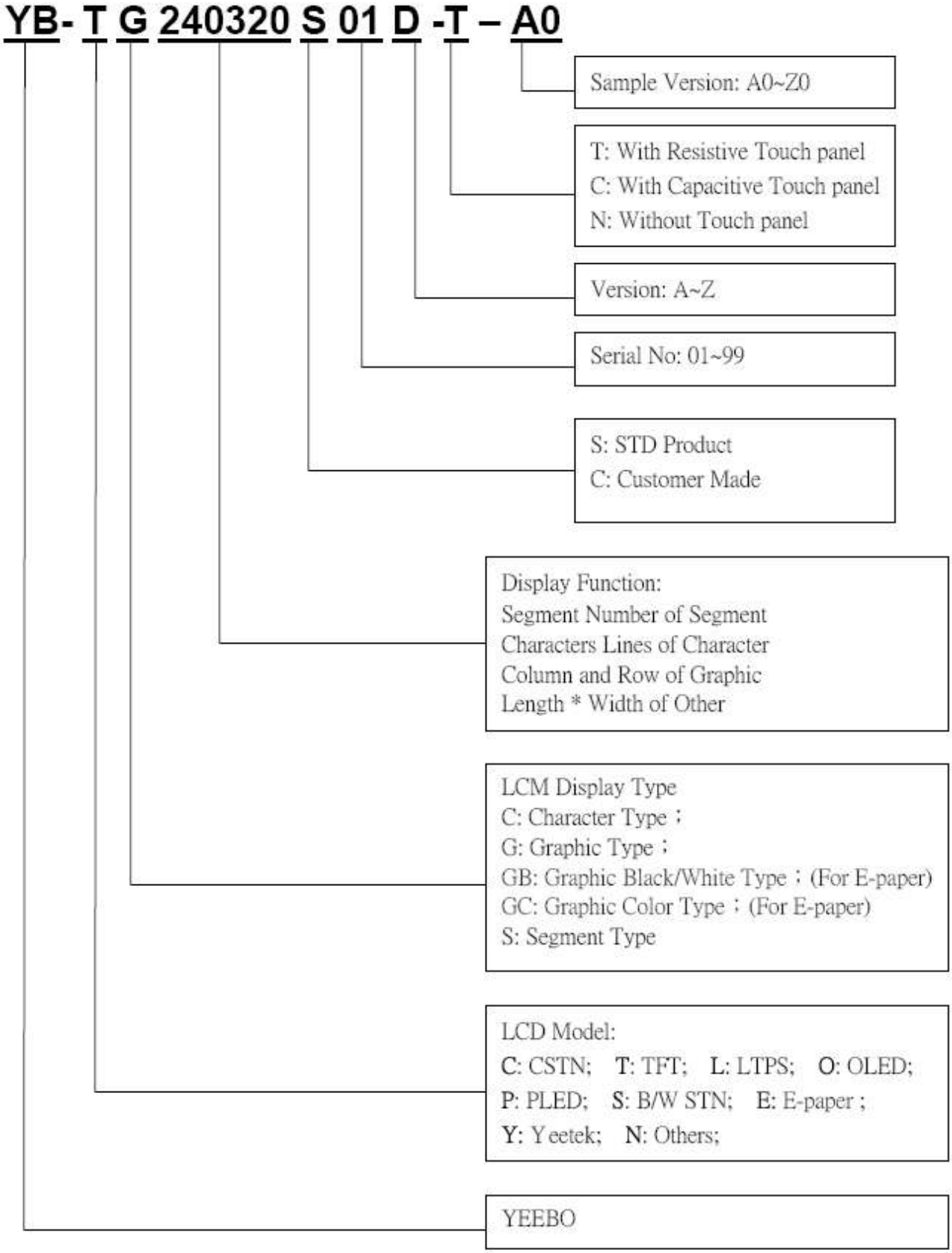
1. Revision History

Sample Version	DOC. Version	DATE	DESCRIPTION		CHANGED BY
C0	00	2019-02-15	FULL SPEC	First Sample	Li

2. Table of Contents:

3. Module Numbering System:

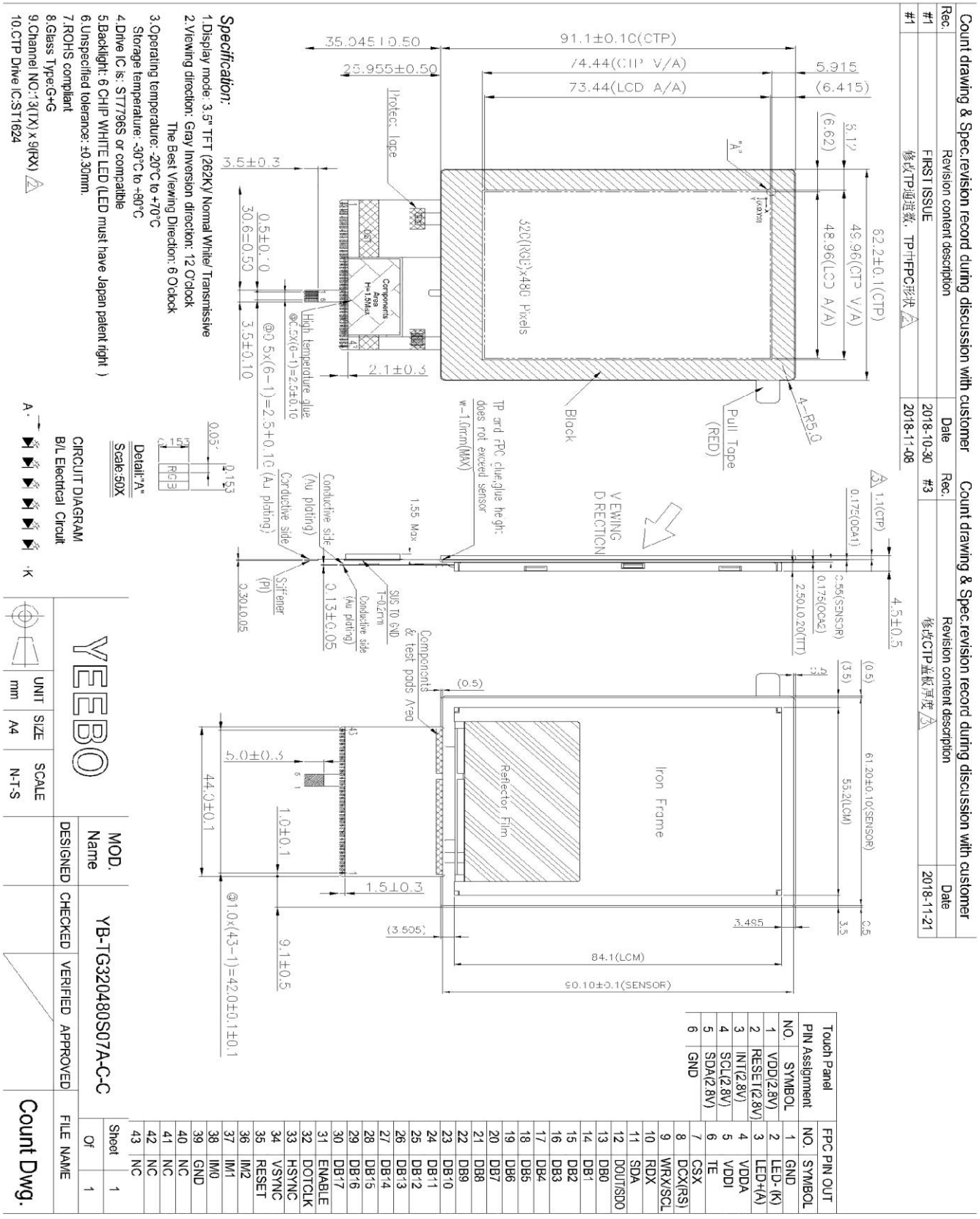
(Example)



4. General Specification:

ITEM	CONTENTS
Module Size	62.2(W) * 91.1(H) * 4.5(T) mm
Module Size(With FPC)	62.2(W) *126.145(H) * 4.5(T) mm
Display Size(Diagonal)	3.5 inch
Display Format	320(RGB) * 480 Pixels
view Area	49.96(W) * 74.44(H) mm
Active Area	48.96(W) * 73.44(H) mm
Pixel Pitch	0.153 * 0.153 mm
LCD Type	TFT(262K) / Transmissive/ NW
View Direction (Gray Inversion)	12:00 O'clock
The Best Viewing Direction:	6:00 O'clock
TP Controller IC	ST1624
TFT Controller IC	ST7796S
Weight	≈50g

5. LCM drawing:

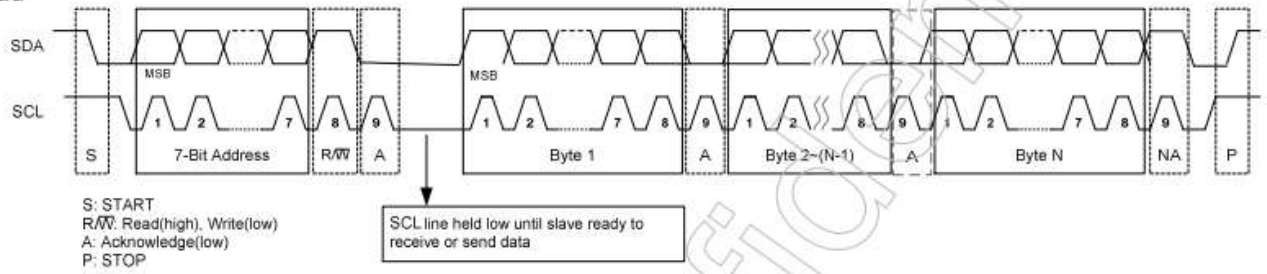


6.DIGITAL INTERFACE

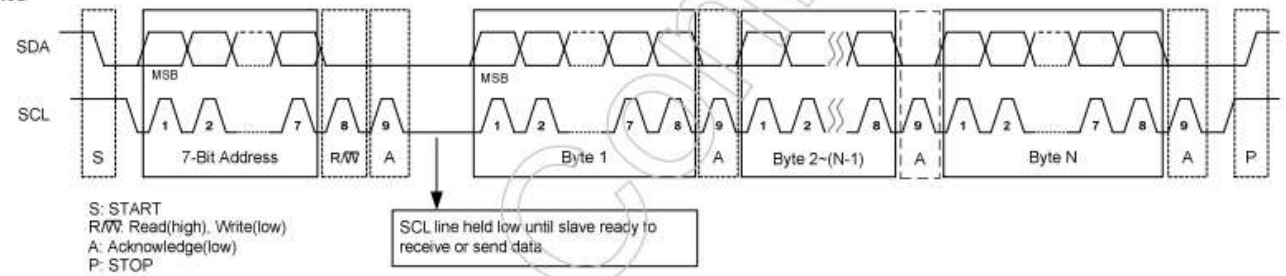
6.1 I2C Slave Interface

ST1624 equipped with I2C provides two wires, serial data (SDA) and serial clock (SCL), to carry transferring information at up to 400 kbit/s(Fast mode). ST1624 plays the slave role in I2C transfer. Both SDA and SCL are bidirectional lines, connected to IOVDD via pull-up resistors. All transactions begin with a START (S) and can be terminated by a STOP (P). 7-bits address follows START to recognize device. Each bye is 8-bits length and followed by an acknowledge bit. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Read



Write



7. Electrical Characteristics

7.1 TP Electrical Characteristics

7.1-1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
VDD	V_{VDD}	-0.3	+6	V
IOVDD	V_{IOVDD}	-0.3	+6	V
Operating Ambient Temperature	T_A	-20	+80	℃
Storage Temperature	T_S	-40	+125	℃

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. All the ranges are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

7.1-2 DC Electrical Characteristics

Condition: VDD = IOVDD = 3.3V, T_A = 25°C, unless be specified individually.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VDD	V_{VDD}	2.7	-	3.6	V	
IOVDD	V_{IOVDD}	1.6	-	3.6	V	
Operating Current	I_{NML}	-	16	24	mA	15TX, 9RX
Idle Current	I_{IDLE}	-	5.9	8.9	mA	15TX, 9RX, scan rate=20Hz
Power Down Current	I_{PD}	-	-	20	uA	
Input High Voltage	V_{IH}	0.85*IOVDD	-	-	V	IOVDD=3.3V
Input Low Voltage	V_{IL}	-	-	0.15*IOVDD	V	IOVDD=3.3V
Input Pull Up Resistor	R_{PU}	50	-	60	KOhm	
Output Driving Current	I_{DRV}	30	-	-	mA	V_{OH} = IOVDD x 0.8
Output Sinking Current	I_{SINK}	80	-	-	mA	V_{OL} = IOVDD x 0.2
Low Voltage Reset	V_{LVR}	-	-	2.3	V	

7.1-3 DC Electrical Characteristics

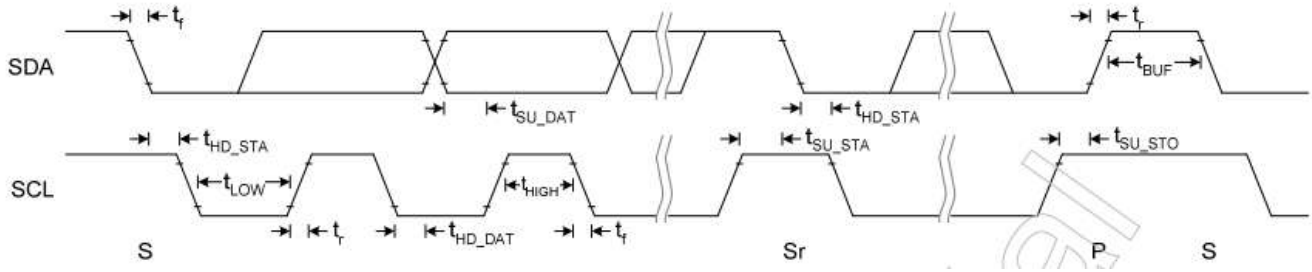


Figure 7-1 IIC Fast Mode Timing

Table 7-3 I2C Fast Mode Timing Characteristic

Conditions: VDD = 3.3V, GND = 0V, T_A = 25°C

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
f_{SCL}	SCL clock frequency	0	-	400	kHz
t_{LOW}	Low period of the SCL clock	1.3	-	-	us
t_{HIGH}	High period of the SCL clock	0.6	-	-	us
t_f	Signal falling time	-	-	300	ns
t_r	Signal rising time	-	-	300	ns
t_{SU_STA}	Set up time for a repeated START condition	0.6	-	-	us
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6	-	-	us
t_{SU_DAT}	Data set up time	100	-	-	ns
t_{HD_DAT}	Data hold time	0	-	0.9	us
t_{SU_STO}	Set up time for STOP condition	0.6	-	-	us
t_{BUF}	Bus free time between a STOP and START condition	1.3	-	-	us
C_b	Capacitive load for each bus line	-	-	400	pF

7.2 LCM Electrical Characteristics

7.2-1 Absolute Maximum Ratings (Ta=25℃ VSS=0V)

Item	Symbol	Min.	Type	Max.	Unit	Remark
Supply Voltage(Analog)	VDDA	-0.3	-	+4.6	V	Note1
Supply Voltage(Logic)	VDDI	-0.3		+4.6		Note1
Logic Input Voltage Range	VIN	0.5		$VDDI_{+0.5}$	V	Note1
Operating Temperature	Topr	-20	-	+70	℃	-
Storage Temperature	Tstg	-30	-	+80	℃	-

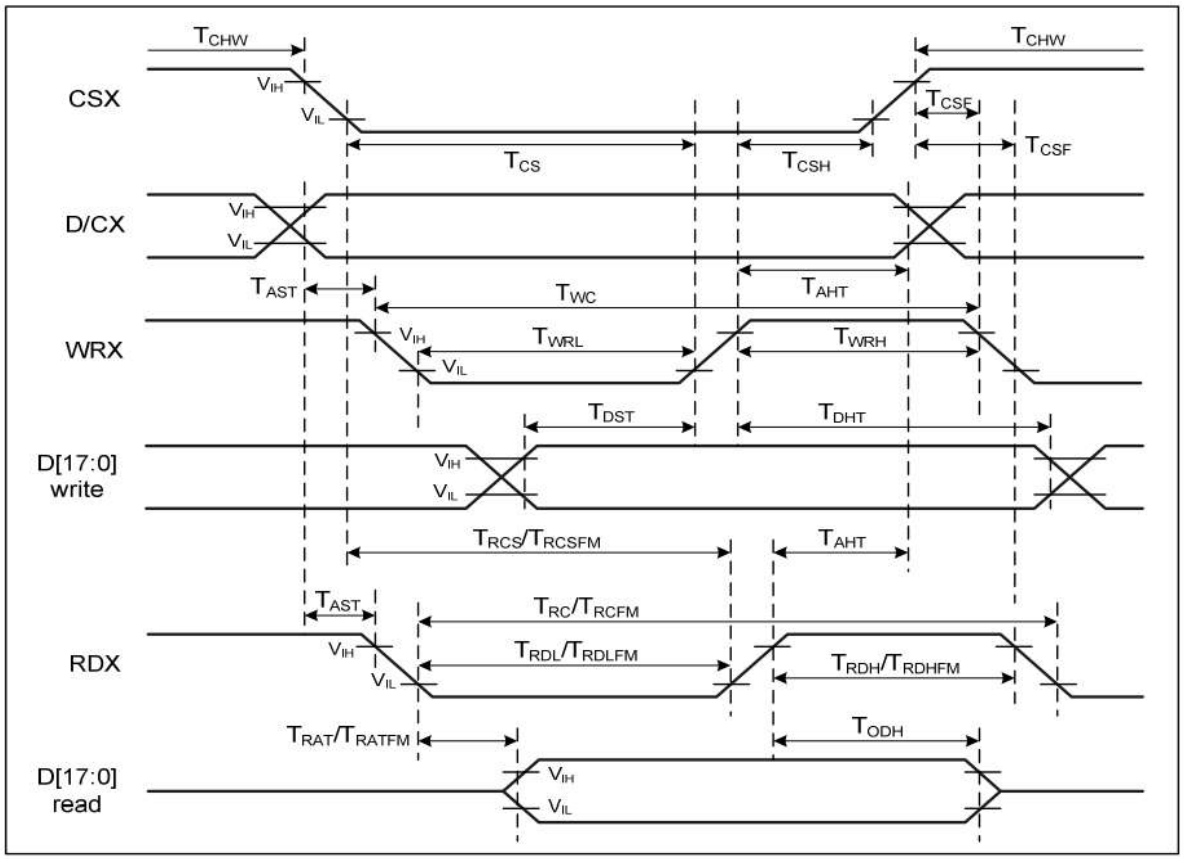
Note1: Absolute maximum rating is the limit value beyond which the IC maybe broken. They do not assure operations.

7.2-2 Operating Conditions (Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply voltage	VDDA&VDDI	-	2.6	2.8	3.0	Volt
Input Voltage	V_{IH}	-	0.7 * VDDI	-	VDDI	V
	V_{IL}	-	VSS	-	0.3* VDDI	V
Power Supply Current for LCM	IDD	VDD=2.8V	-	17	25.5	mA

7.2-3 Timing Characteristics

8080 Series MCU Parallel interface Characteristics:18/16/9/8-bir Bus



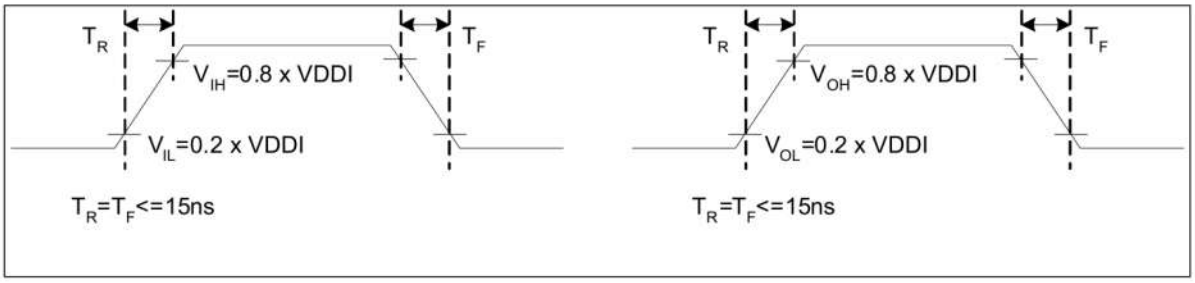
Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	

	T_{WRL}	Control pulse “L” duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	20	80	ns	

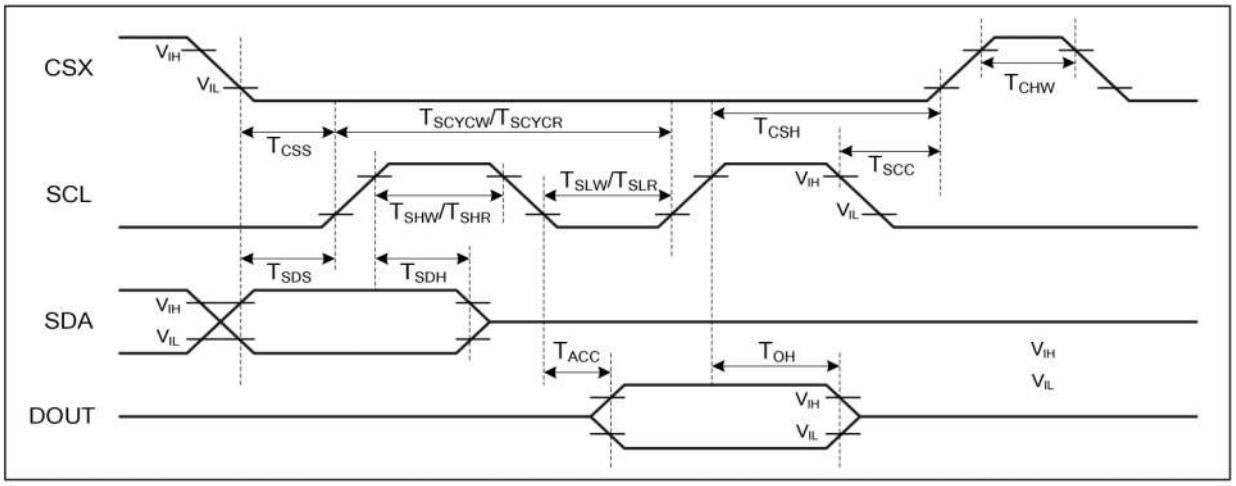
8080 Parallel Interface Characteristics



Rising and Falling Timing for I/O Signal

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

3-SPI Serial Data Transfer Interface Characteristics:



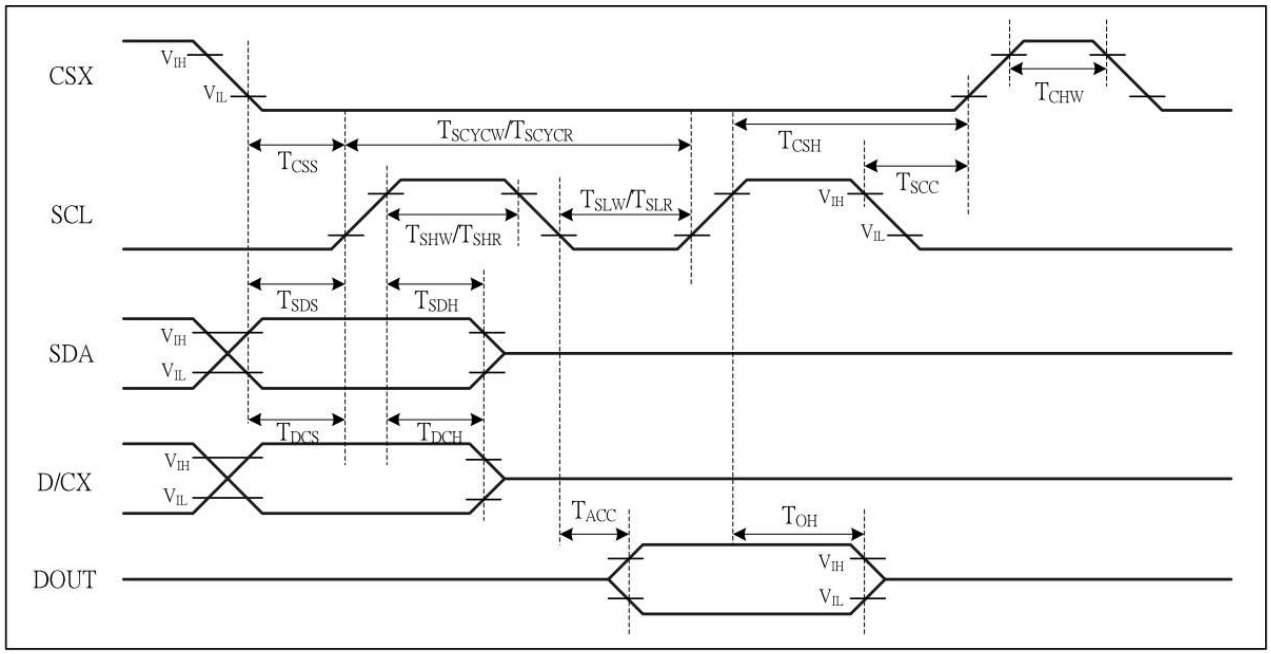
3-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-SPI Interface Characteristics

4-SPI Serial Data Transfer Interface Characteristics

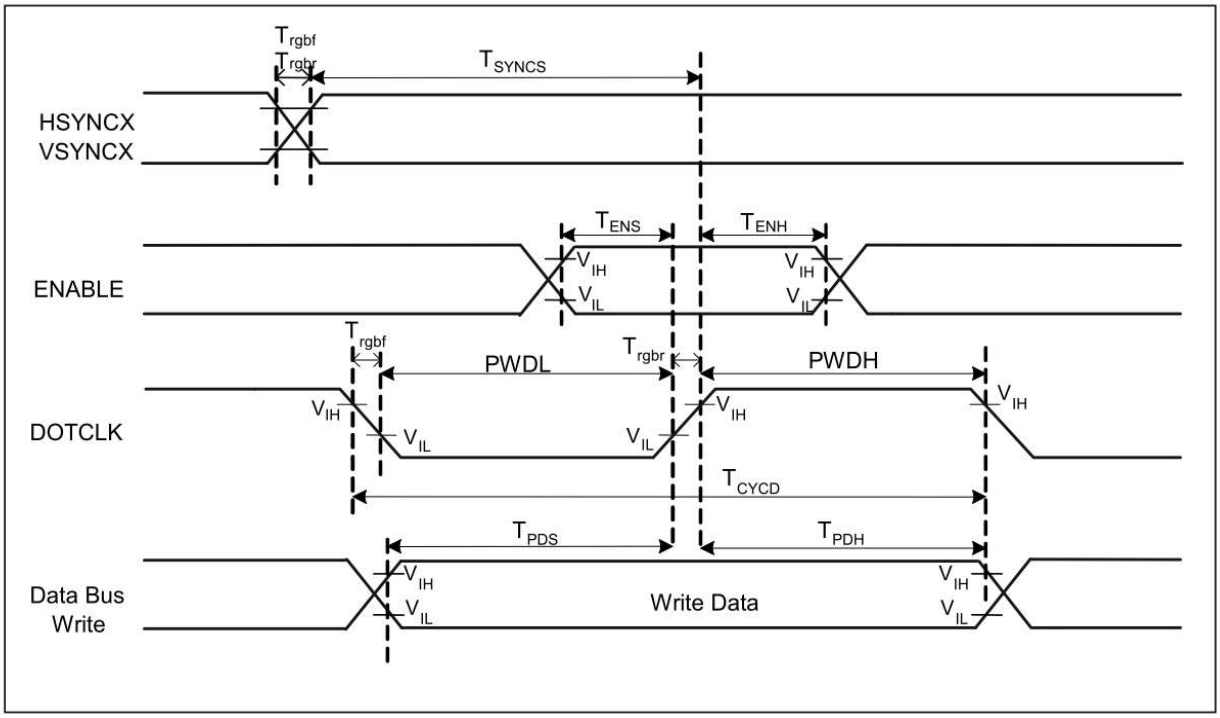


4-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

RGB Interface Characteristics:



VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	30	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	30	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	66	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

RGB Interface Timing Characteristics

7.3. Optical Characteristics:

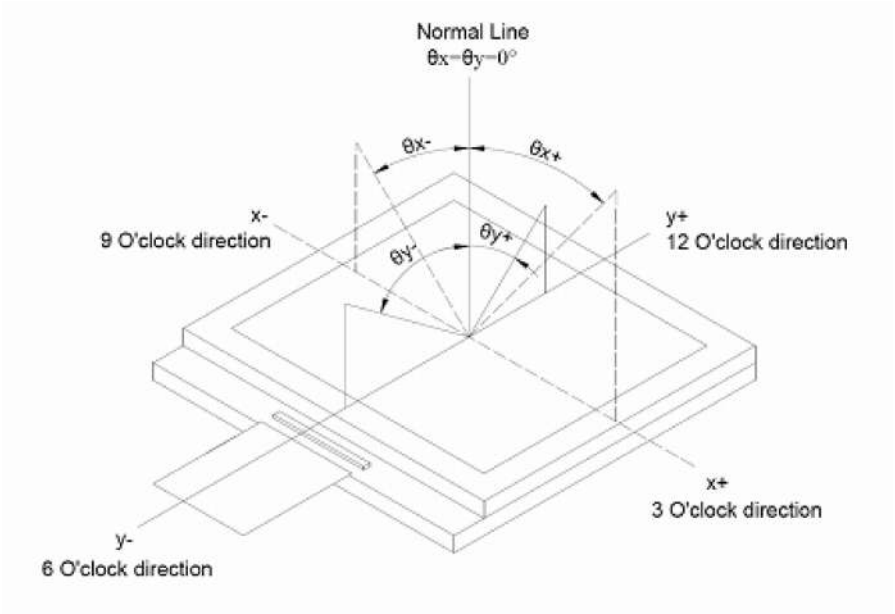
Item		Symbol	Conditions	Specifications			Unit	Note
				Min	Typ	Max		
Transmittance (With PL)		T(%)	-	-	5.5	-	-	-
Contrast Ratio		CR	Θ=0 Normal Viewing angle	-	500	-		(1) (2)
Response time		TR+TF	-	-	16	-	ms	(1) (3)
Viewing angle	Hor.	ΘX+	CR≧10	-	70	-	deg.	-
		ΘX-		-	70	-		
	Ver.	Θy+		-	70	-		
		Θy-		-	60	-		

Measuring Condition
1. Measuring surrounding: dark room
2. Ambient temperature: 25±2℃
3. 30 min. Warm-up time.

Color of CIE Coordinate:

Item		Symbol	Condition	Min.	Typ.	Max.
Chromaticity Coordinates (Transmissive)	Red	x	θ = ϕ = 0° LED Backlight	0.555	0.605	0.655
		y		0.31	0.36	0.41
	Green	x		0.274	0.324	0.374
		y		0.519	0.569	0.619
	Blue	x		0.095	0.145	0.195
		y		0.050	0.100	0.150
	White	x		0.249	0.299	0.349
		y		0.265	0.315	0.365

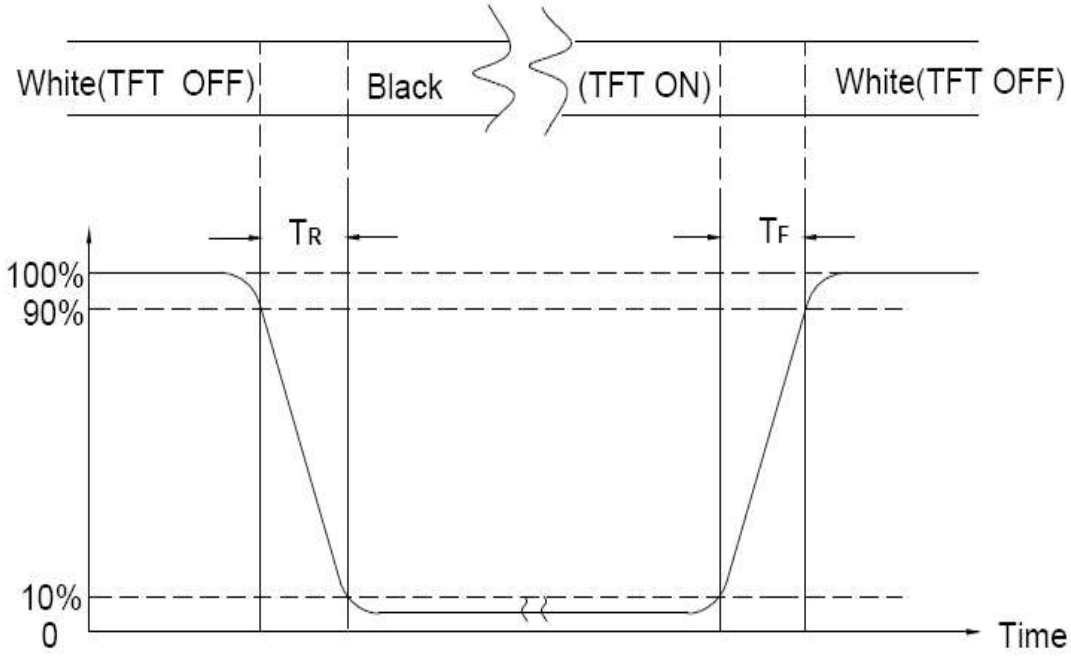
Note (1) Definition of Viewing Angle :



Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black}}$$

Note (3) Definition of Response Time : Sum of TR and TF



8. Interface Pin Assignment:

8-1 LCM FPC Interface

No.	Symbol	Function
1	GND	Power Ground.
2	LED- (K)	Cathode of LED Backlight.
3	LED+ (A)	Anode of LED Backlight.
4	VDDA	Power Supply for Analog.
5	VDDI	Power supply for I/O system.
6	TE	Tearing effect output. If not used. leave this pin open.
7	CSX	Chip select signal.
8	DCX(RS)	Display data/command selection (RS) pin in MCU interface. DCX=1: display data or parameter. DCX=0: register index / command.
9	WRX/SCL	Write enable in MCU parallel interface. In SPI mode, this pin is used as SCL.
10	RDX	Read enable in 8080 MCU parallel interface. Low-active.
11	SDA	SPI interface input/output pin. The data is latched on the rising edge of the SCL signal. If not used, please fix this pin at VDDI or GND level.
12	DOUT/SDO	SPI interface output pin. The data is outputted on the falling edge of the SCL signal. If not used, please fix this pin at floating.
13	DB0	Data Bus.
14	DB1	
15	DB2	
16	DB3	
17	DB4	
18	DB5	
19	DB6	
20	DB7	
21	DB8	
22	DB9	

No.	Symbol	Function
23	DB10	Data Bus.
24	DB11	
25	DB12	
26	DB13	
27	DB14	
28	DB15	
29	DB16	
30	DB17	
31	ENABLE	Data enable signal for RGB interface operation. If not used, please fix this pin at VDDI or GND.
32	DOTCLK	Dot clock signal for RGB interface operation. If not used, please fix this pin at VDDI or GND.
33	HSYNC	Horizontal synchronizing input signal for RGB interface operation. If not used, please fix this pin at VDDI or GND.
34	VSYNC	Vertical synchronizing input signal for RGB interface operation. If not used, please fix this pin at VDDI or GND.
35	RESET	Reset pin.
36	IM2	The interface mode select. Note1
37	IM1	
38	IM0	
39	GND	Power Ground.
40	NC(YU)	Open.
41	NC(XL)	Open.
42	NC(YD)	Open.
43	NC(XR)	Open.

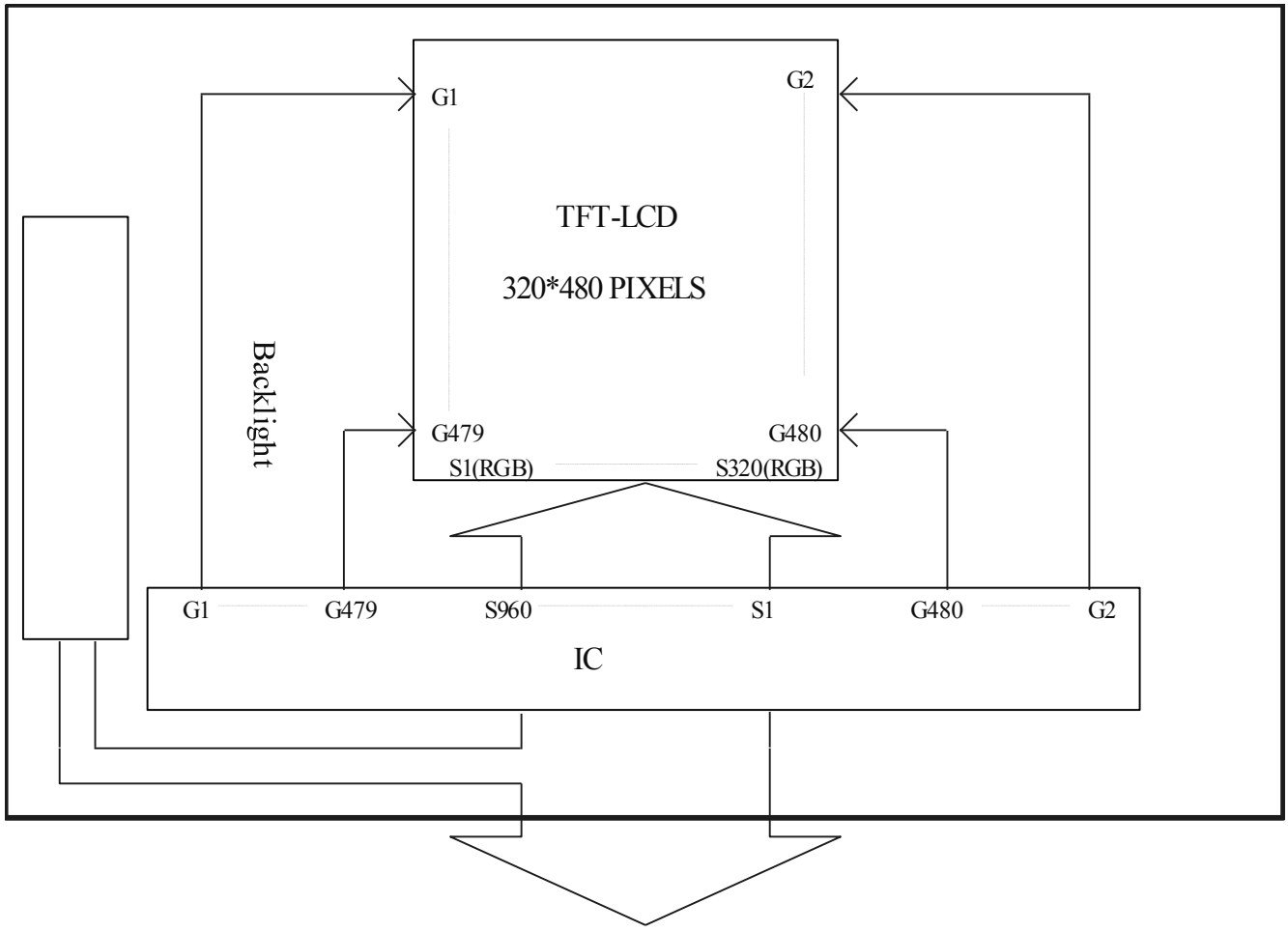
Note 1:

IM2	IM1	IM0	MPU Interface Mode	Data pin
0	0	0	8080 18-bit Interface	DB[17:0]
0	0	1	8080 9-bit Interface	DB[8:0]
0	1	0	8080 16-bit Interface	DB[15:0]
0	1	1	8080 8-bit Interface	DB[7:0],
1	0	0	Reserve	--
1	0	1	3SPI	SDA, SDO
1	1	0	Reserve	--
1	1	1	4Line SPI	SDA, SDO

8-2 TP FPC Interface:

No.	Symbol	Function
1	VDD	CTP Power Voltage for digital circuit
2	RESET	Reset low (For CTP), Connection to host system is recommended
3	INT	State change Interrupt Note: Briefly set (~100 ms) as an input afterpower-up/reset for diagnostic purposes
4	SCL	I^2C Serial Clock
5	SCL	I^2C Serial Clock
6	GND	Power Ground.

9. Block Diagram:



10. Backlight:

1. Standard Lamp Styles (Edge Lighting Type):
The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption:

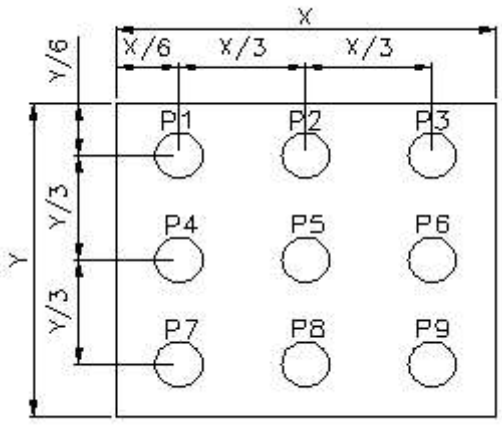
2. The Main Advantages of the LED Backlight are as following:
2.1 The brightness of the backlight can simply be adjusted.
By a resistor or a potentiometer.

3. Data About LED Backlight: (Ta=25℃)

PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
Supply Current	I	-	20	-	mA	V=17.4V	
Supply Voltage	V	16.5	17.4	18.6	V	If=20mA	
Luminous Intensity for LCM	IV	180	250	-	cd/m^2		2
Uniformity for LCM	-	70	-	-	%		3
Life Time	-	20000	50000	-	Hr.		4
Color	White						

NOTE:
1. Backlight Only
2. Average Luminous Intensity of P1-P9
3. Uniformity = Min/Max * 100%
4. LED life time defined as follows: The final brightness is at 50% of original brightness

Measured Method: (X*Y: Light Area)



Internal Circuit Diagram

(Effective spatial Distribution)
Hole Diameter ø3 mm; 1 to 9 per Position Measured Luminous

11. Standard Specification for Reliability:

11–1. Standard Specifications for Reliability of LCD Module

No	Item	Description
01	High temperature operation	The sample should be allowed to stand at 70℃ for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
02	Low temperature operation	The sample should be allowed to stand at -20℃ for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
03	High temperature storage	The sample should be allowed to stand at 80℃ for 240 hours under no-load condition, and then returning it to normal temperature condition, and allowing it stand for 2 hours.
04	Low temperature storage	The sample should be allowed to stand at -30℃ for 240 hours under no-load condition, then returning it to normal temperature condition, and allowing it stand for 2 hours.
05	Moisture storage	The sample should be allowed to stand at 60℃,90%RH MAX for 240 hours under no-load condition, then taking it out and drying it at normal temperature for 2 hours.
06	Thermal shock storage	The sample should be allowed to stand the following 10 cycles : -30℃ for 30 minutes → normal temperature for 5 minutes → +80℃ for 30 minutes → normal temperature for 5 minutes, as one cycle.
07	Packing vibration	Frequency range : 10Hz ~ 55Hz Amplitude of vibration : 1.5mm Sweep time: 12 min X,Y,Z 2 hours for each direction.
08	Packing drop test	According to ISTA 1A 2001.

*Sample size for each test item is 3~5pcs

11 - 2. Testing Conditions and Inspection Criteria

For the final test the testing sample must be stored at room temperature for 24 hours, after the tests listed in Table 11.2, Standard specifications for Reliability have been executed in order to ensure stability.

No	Item	Test Model	In section Criteria
01	Current Consumption	Refer To Specification	The current consumption should conform to the product specification.
02	Contrast	Refer To Specification	After the tests have been executed, the contrast must be larger than half of its initial value prior to the tests.
03	Appearance	Visual inspection	Defect free.

11- 3. MTBF

MTBF	Functions, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (25±5℃), normal humidity (50±10% RH), and in area not exposed to direct sun light.

12. Specification of Quality Assurance:

12-1. Purpose

This standard for Quality Assurance should affirm the quality of LCD module products to supply to purchaser by YEEBO CORPORATION (Supplier).

12-2. Standard for Quality Test

a. Inspection:
Before delivering, the supplier should take the following tests, and affirm the quality of product.

b. Electro-Optical Characteristics:
According to the individual specification to test the product.

c. Test of Appearance Characteristics:
According to the individual specification to test the product.

d. Test of Reliability Characteristics:
According to the definition of reliability on the specification for testing products.

e. Delivery Test:
Before delivering, the supplier should take the delivery test.
(i) Test method: According to **ISO2859-1**.General Inspection Level Ⅱ take a single time.
(ii) The defects classify of AQL as following:
Major defect: AQL = 0.65
Minor defect: AQL = 2.5
Total defects: AQL = 2.5

12-3. Non- conforming Analysis & Deal With Manners

a. Non- conforming Analysis:
(i) Purchaser should supply the detail data of non- conforming sample and the non-conforming.
(ii) After accepting the detail data from purchaser, the analysis of non- conforming should be finished in two weeks.
(iii) If supplier can not finish analysis on time, must announce purchaser before 3 days.

b. Disposition of non- conforming:
(i) If find any product defect of supplier during assembly time, supplier must change the good product for every defect after recognition.
(ii) Both supplier and customer should analyze the reason and discuss the disposition of non-conforming when the reason of nonconforming is not sure.

12-4. Agreement items

Both sides should discuss together when the following problems happen.

a. There is any problem of standard of quality assurance, and both sides should think that must be modified.
b. There is any argument item which does not record in the standard of quality assurance.
c. Any other special problem.

12-5. Standard of The Product Appearance Test

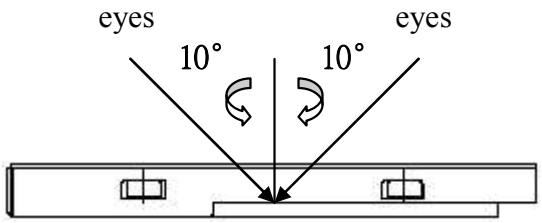
a. Manner of appearance test:

(i) The test must be under 20W × 2 or 40W fluorescent light, and the distance of view must be at 30±5cm.

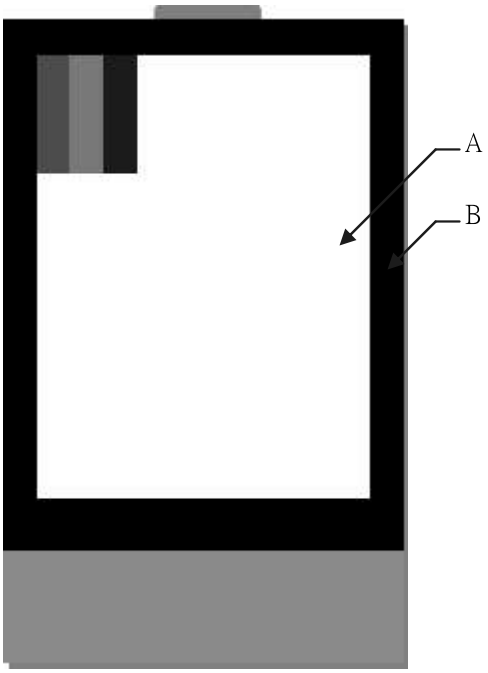
(ii) When test the model of transmissive product must add the reflective plate.

(iii)The test direction is base on around 10° of vertical line.

(iiii)Temperature: 25±5℃ Humidity: 60±10%RH



(iv) Definition of area:



A. Area: Viewing area.

B. Area: Out of viewing area.
(Outside viewing area)

b. Basic principle:

(i) It will accord to the AQL when the standard can not be described.

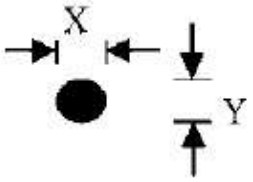
(ii) The sample of the lowest acceptable quality level must be discussed by both supplier and customer when any dispute happened.

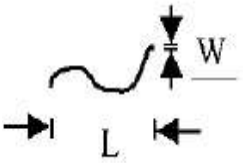
(iii) Must add new item on time when it is necessary.

c. Standard of inspection: (Unit: mm)

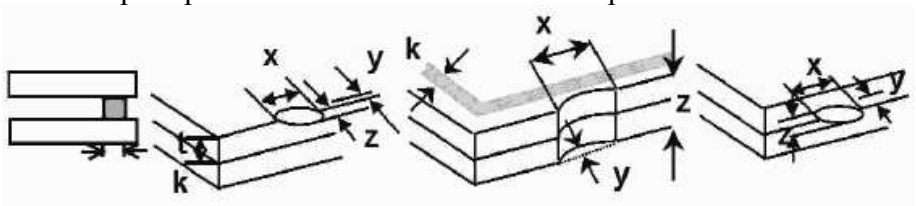
12-6. Inspection specification

Defect out of viewing area can be neglected.

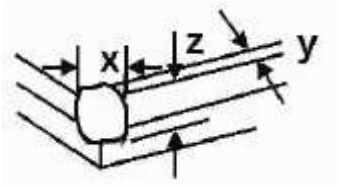
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character, dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 LCD viewing angle defect.
1.7 Mixed product types.
1.8 Flicker</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or White spots or Bright spots or Color spots on LCD (Display only)</td><td>2.1 White and black or color spots on display ≦ 0.25mm, no more than Five spots.
2.2 Densely spaced: No more than three spots within 3mm.</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">LCD and Touch Panel black spots, white spots, contamination (non – display)</td><td>3.1 Round type: As following drawing
Φ = (X+Y) / 2
 

<table>
<tr><th>Size(mm)</th><th>Acceptable Q'ty</th></tr>
<tr><td>Φ≦0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20< Φ≦0.50</td><td>2</td></tr>
<tr><td>0.5< Φ≦0.75</td><td>2</td></tr>
<tr><td>0.5< Φ≦1.0</td><td>1</td></tr>
<tr><td>1.0< Φ</td><td>0</td></tr>
</table>
* Densely spaced: No more than two spots within 3mm.</td><td>2.5</td></tr>
<tr><td>3.2 Line type: (As following drawing)
 

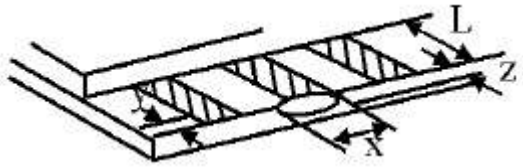
<table>
<tr><th>Length(mm)</th><th>Width(mm)</th><th>Acceptable Q'ty</th></tr>
<tr><td>---</td><td>W≦0.05</td><td>Accept no dense</td></tr>
<tr><td>L≦5.0</td><td>0.05<W≦0.10</td><td rowspan="2">2</td></tr>
<tr><td>L≦5.0</td><td>0.10<W≦0.15</td></tr>
<tr><td>---</td><td>0.15<W</td><td>Rejection</td></tr>
</table>
* Densely spaced: No more than two lines within 3mm.</td><td>2.5</td></tr>
</table>

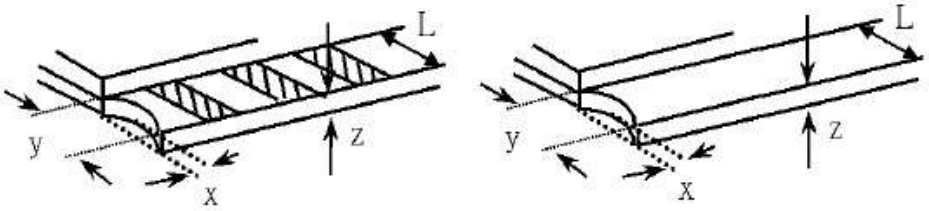
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction
<table>
<tr><td>Size Φ(mm)</td><td>Acceptable Q'ty</td></tr>
<tr><td>Φ≦0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20< Φ≦0.50</td><td>3</td></tr>
<tr><td>0.50< Φ≦1.00</td><td>2</td></tr>
<tr><td>1.00< Φ</td><td>0</td></tr>
<tr><td>Total Q’ty</td><td>3</td></tr>
</table></td><td>2.5</td></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 -2 Line Type.</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>Symbols:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: LCD side length
L: Electrode pad length
6.1 General glass chip:
6.1.1 Chip on panel surface and crack between panels:
 

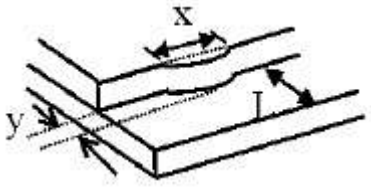
<table>
<tr><td>z: Chip thickness</td><td>y: Chip width</td><td>x: Chip length</td></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t< z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙ Unit: mm
⊙ If there are 2 or more chips, x is the total length of each chip

6.1.2 Corner crack:
 

<table>
<tr><td>z: Chip thickness</td><td>y: Chip width</td><td>x: Chip length</td></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t< z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙ Unit: mm
⊙ If there are 2 or more chips, x is the total length of each chip</td><td>2.5</td></tr>
</table>

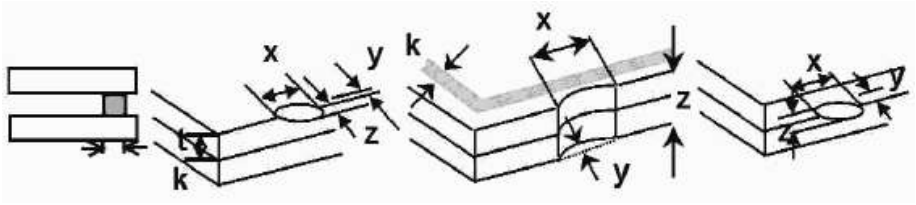
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>07</td><td>Glass crack</td><td>
Symbols:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: LCD side length
L: Electrode pad length
7.2 Protrusion over terminal:
7.2.1 Chip on electrode pad:


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦0.5mm</td><td>x≦1/8a</td><td>0< z≦t</td></tr>
</table>
7.2.2
Non-conductive portion:


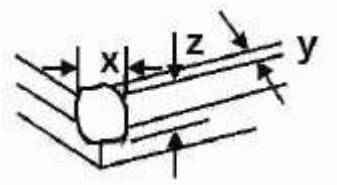
<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦L</td><td>x≦1/8a</td><td>0< z≦t</td></tr>
</table>
⊙ If there chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.
⊙ If the product will be heat sealed by the customer, the alignment mark must mot be damaged.
7.2.3 Substrate protuberance and internal crack


<table>
<tr><th>y: width</th><th>x: length</th></tr>
<tr><td>y≦1/3L</td><td>X≦a</td></tr>
</table>
</td><td>2.5</td></tr>
</table>

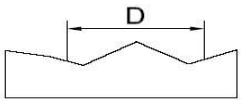
NO	Item	Criterion	AQL
08	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
09	Backlight elements	9.1 Illumination source flickers when lit. 9.2 Spots or scratches that appear when lit must be judged. Using LCD spot, lines and contamination standards. 9.3 Backlight doesn't light or color is wrong.	2.5 2.5 0.65
10	Bezel	Bezel must comply with product specifications.	2.5
11	PCB、COB	11.1 COB seal may not have pinholes larger than 0.2mm or contamination. 11.2 COB seal surface may not have pinholes through to the IC. 11.3 The height of the COB should not exceed the height indicated in the assembly diagram. 11.4 There may not be more than 2mm of sealant outside the seal area on PCB. And there should be no more than three places. 11.5 Parts on PCB must be the same as on the production characteristic chart, There should be no wrong parts, missing parts or excess parts. 11.6 The jumper on the PCB should conform to the product characteristic chart.	2.5 2.5 2.5 2.5 0.65 0.65
12	FPC	12.1 FPC terminal damage ≦ 1/2 FPC terminal width and can not affect the function , we judge accept. 12.2 FPC alignment hole damage ≦ 1/2 alignment area and can not affect the function , we judge accept.	2.5 2.5
13	Soldering	13.1 No cold solder joints, missing solder connections, oxidation or icicle. 13.2 No short circuits in components on PCB or FPC.	2.5 0.65

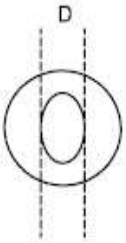
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>14</td><td>Touch Panel Chipped glass</td><td>
Symbols:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Touch Panel Total thickness a: LCD side length
L: Electrode pad length
14.1 General glass chip:
14.1.1 Chip on panel surface and crack between panels:


<table>
<tr><td>z: Chip thickness</td><td>y: Chip width</td><td>x: Chip length</td></tr>
<tr><td>Z≦t</td><td>≦1/2 k and not over viewing area</td><td>x≦1/8a</td></tr>
</table>
⊙ Unit: mm
⊙ If there are 2 or more chips, x is the total length of each chip

14.1.2 Corner crack:


<table>
<tr><td>z: Chip thickness</td><td>y: Chip width</td><td>x: Chip length</td></tr>
<tr><td>z≦t</td><td>≦1/2 k and not over viewing area</td><td>x≦1/8a</td></tr>
</table>
⊙ Unit: mm
⊙ If there are 2 or more chips, x is the total length of each chip
</td><td>2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>15</td><td>Touch Panel(Fish eye、dent and bubble on film)</td><td>
<table>
<tr><th>SIZE(mm)</th><th>Acceptable Q’ty</th></tr>
<tr><td>Φ≦0.2</td><td>Accept no dense</td></tr>
<tr><td>0.2< D ≦0.4</td><td>5</td></tr>
<tr><td>0.4< D ≦0.5</td><td>2</td></tr>
<tr><td>0.5< D</td><td>0</td></tr>
</table>




</td><td>2.5</td></tr>
<tr><td>16</td><td>Touch Panel Newton ring</td><td>Newton ring dimension ≦ 1/2 touch panel area and not affect font and line distortion(≦2.5%) , it is acceptable.</td><td>2.5</td></tr>
<tr><td>17</td><td>Touch Panel Linearity</td><td>Less than 2.5% is acceptable.</td><td>2.5</td></tr>
<tr><td>18</td><td>LCD Ripple</td><td>Touch the touch panel , can not see the LCD ripple.
Pen: R 1.0mm silicon rubber.
Operation Force: 80g</td><td>2.5</td></tr>
<tr><td>19</td><td>General appearance</td><td>19.1 Pin type must match type in specification sheet.
19.2 LCD pin loose or missing pins.
19.3 Product packaging must the same as specified on packaging specification sheet.
19.4 Product dimension and structure must conform to product specification sheet.</td><td>0.65
0.65
0.65
0.65</td></tr>
</table>

13. Handling Precaution:

13-1 Handling of LCM

- Don't give external shock.
- Don't apply excessive force on the surface.
- Liquid in LCD is hazardous substance. Must not lick and swallow. when the liquid is attach to your hand, skin, cloth etc. Wash it out thoroughly and immediately.
- Don't operate it above the absolute maximum rating.
- Don't disassemble the LCM.
- The operators should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads,the copper leads on the PCB and the interface terminals with any parts of the human body.
- The modules should be kept in antistatic bags or other containers resistant to static for storage.
- The module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

13-2 Storage

- Store in an ambient temperature of 25±10℃, and in a relative humidity of 50±10%RH. Don't expose to sunlight or fluorescent light.
- Storage in a clean environment, free from dust, active gas, and solvent.
- Store in anti-static electricity container.
- Store without any physical load.

13-3 Soldering

- Use only soldering irons with proper grounding and no leakage.
- Iron: No higher than 280±10℃ and less than 3 sec during Hand soldering.
- Rewiring: no more than 2 times.

14. Guarantee:

Our products could meet requirements of the environment.
YB's RoHS is introduce European Union Directive 2011/65/EU (ROHS)
Requirements and Update.