SPECIFICATION
FOR
CTP MODULE

MODULE NO: YB-TG4801280S02A-C-A0

Doc.Version:00

Customer Approval:

□ Accept	□ Reject

YEEBO	NAME	SIGNATURE	DATE
Prepare	Electronic Engineer	赵春凤	2022-08-31
Check	Mechanical Engineer	李毅斌	2022-09-02
Verify			2022-09-02
Approval			2022-09-02

■ APPROVAL FOR SPECIFICATIONS ONLY

□ APPROVAL FOR SPECIFICATIONS AND SAMPLE

WIMRD005-02-D

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1. Revision History

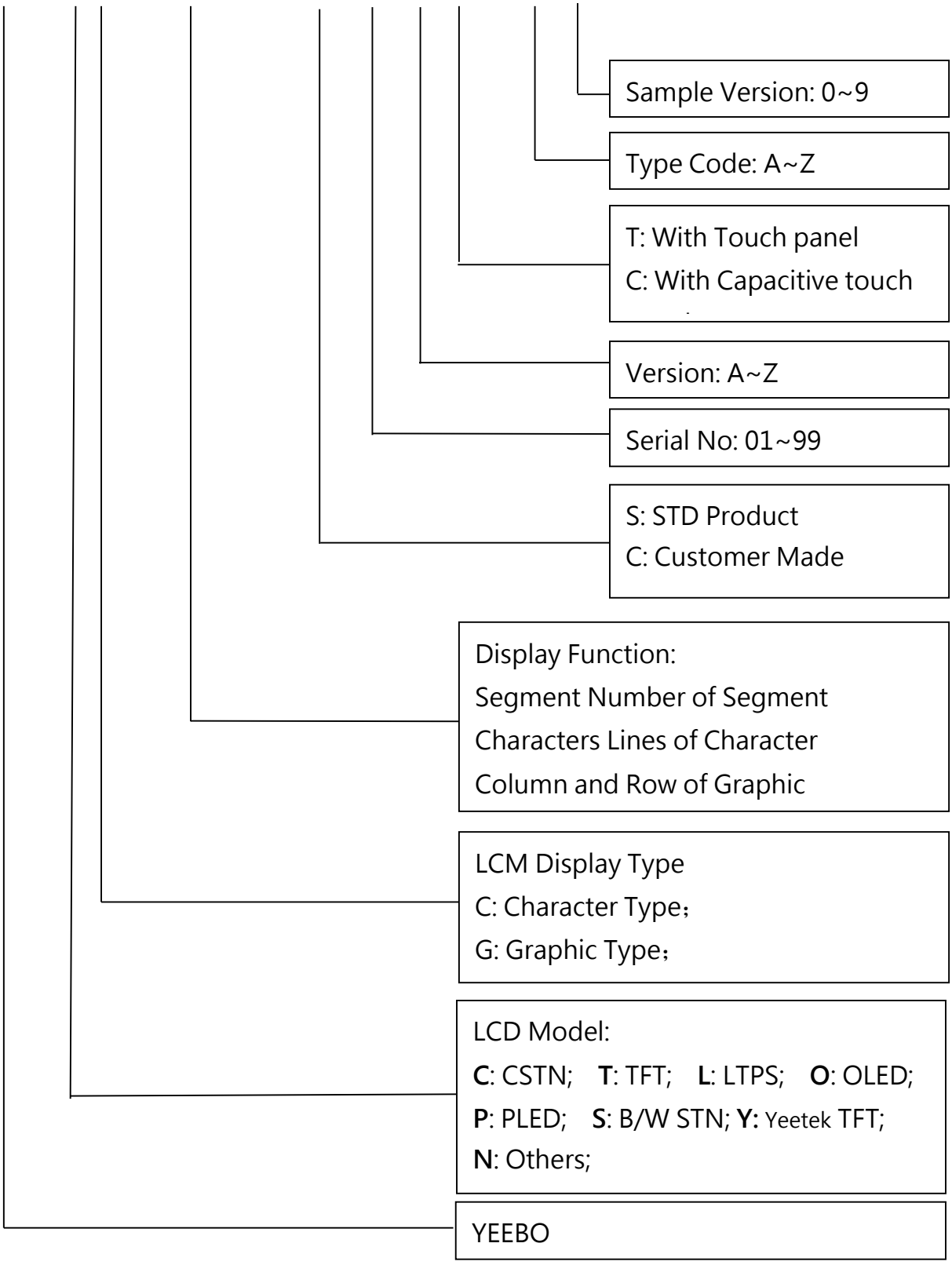
Sample Version	DOC. Version	DATE	DESCRIPTION		CHANGED BY
A0	00	2022-08-31	SPEC ONLY	First issue	ZCF

2. Table of Contents

3. Module Numbering System

(Example)

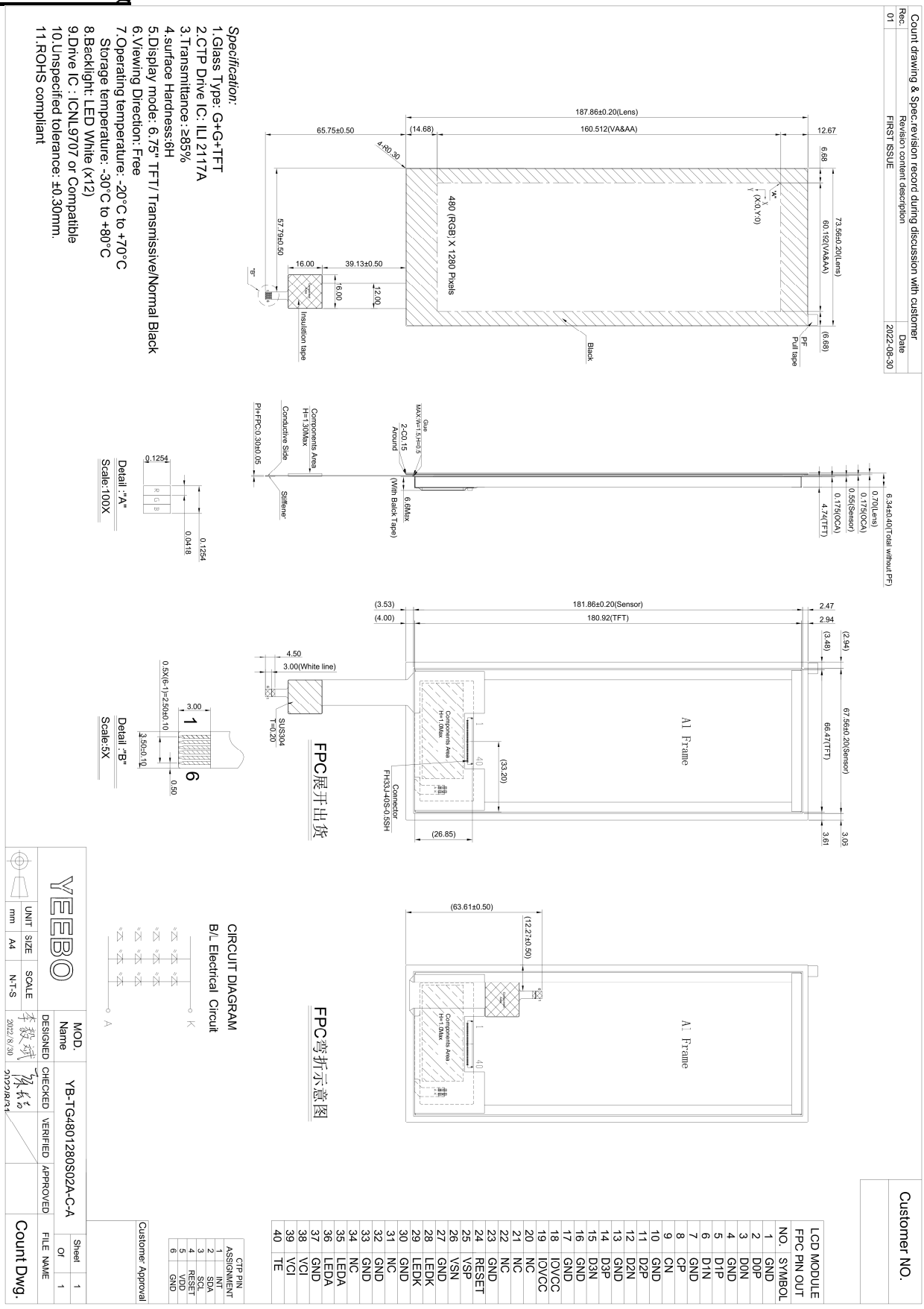
YB- TG 4801280 S 02 A-C – A 0



4. General Specification

ITEM	CONTENTS
Module Size	73.56 (W) * 187.86 (H) * 6.34(T) mm
Module Size (with FPC)	73.56 (W) * 253.61 (H) * 6.34(T) mm
Display Size (Diagonal)	6.75 inch
Display Format	480(RGB)* 1280 Pixels
Active Area	60.192 (W) * 160.512 (H) mm
View Area	60.192 (W) * 160.512 (H) mm
Pixel Pitch	0.1254 * 0.1254 mm
LCD Type	TFT (16.7M)/ Transmissive / Normal Black
The Best Viewing Direction	Free
Controller IC	ICNL9707
CTP IC	ILI2117A
Weight	TBD

5. Drawing


Count drawing & Spec.revision record during discussion with customer
Rec. 01
Revision content description
FIRST ISSUE
Date
2022-08-30
Specification:
1.Glass Type: G+G+TFT
2.CTP Drive IC: ILI 2117A
3.Transmittance : ≥85%
4.surface Hardness:6H
5.Display mode: 6.75" TFT/ Transmissive/Normal Black
6.Viewing Direction: Free
7.Operating temperature: -20°C to +70°C
Storage temperature: -30°C to +80°C
8.Backlight: LED White (x12)
9.Drive IC : ICNL9707 or Compatible
10.Unspecified tolerance: ±0.30mm.
11.ROHS compliant
187.86±0.20(Lens)
160.512(VA&AA)
65.75±0.50
(14.68)
12.67
6.68
4-R0.30
480 (RGB) X 1280 Pixels
(X,0) (Y,0)
73.56±0.20(Lens)
60.192(VA&AA)
57.79±0.50
16.00
39.13±0.50
6.00
2.00
(6.68)
Insulation tape
Black
PF
Pull tape
Glue
MAX:W=1.5,H=0.5
Components Area
H=1.30Max
Conductive Side
PI+FPC:0.30±0.05
2-C0.15
Around
Stiffener
(With Balck Tape)
6.6Max
0.70(Lens)
0.175(OCA)
0.55(Sensor)
0.175(OCA)
4.74(TFT)
6.34±0.40(Total without PF)
Detail :"A"
Scale:100X
0.1254
0.0418
FPC展开出货
(3.53)
(4.00)
181.86±0.20(Sensor)
180.92(TFT)
2.47
2.94
(3.48)
(2.94)
4.50
3.00(White line)
SUS304
T=0.20
Components Area
H=1.0Max
Al Frame
67.56±0.20(Sensor)
66.47(TFT)
(33.20)
Connector
FH33J-40S-0.5SH
(26.85)
3.61
3.05
Detail :"B"
Scale:5X
0.5X(6-1)=2.50±0.10
3.00
3.50±0.10
0.50
FPC弯折示意图
(63.61±0.50)
(12.21±0.50)
CIRCUIT DIAGRAM
B/L Electrical Circuit
A
K
LCD MODULE
FPC PIN OUT
NO. SYMBOL
1 GND
2 D0P
3 D0N
4 GND
5 D1P
6 D1N
7 GND
8 CP
9 CN
10 GND
11 D2P
12 D2N
13 GND
14 D3P
15 D3N
16 GND
17 GND
18 IOVCC
19 IOVCC
20 NC
21 NC
22 NC
23 GND
24 RESET
25 VSP
26 VSN
27 GND
28 LEDK
29 LEDK
30 GND
31 NC
32 GND
33 GND
34 NC
35 LEDA
36 LEDA
37 GND
38 VCI
39 VCI
40 TE
CTP PIN ASSIGNMENT
1 INT
2 SDA
3 SCL
4 RESET
5 VDD
6 GND
Customer Approval
Customer NO.
YEEBO
UNIT mm
SIZE A4
SCALE N.T-S
MOD. Name
YB-TG4801280S02A-C-A
DESIGNED 李毅武 2022/8/20
CHECKED 2022/8/21
VERIFIED
APPROVED
FILE NAME Count Dwg.
Sheet 1
Of 1

6. Electrical Characteristics

6-1 Absolute Maximum Ratings

6-1-1 Absolute Maximum Ratings (TFT) (Ta=25℃ VSS=0V)

Item	Symbol	Min.	Type	Max.	Unit	Remark
Power Supply voltage	IOVCC ~ VSSD	-0.3	-	3.3	Volt	
	VCC ~ VSSA	-0.3	-	6.6	Volt	
	HS_VCC ~ HS_VSS	-0.3	-	3.3	Volt	
	VSP ~ VSSA	-0.3	-	6.6	Volt	
	VSSA ~ VSN	-6.6	-	0	Volt	
	VGH ~ VGL	|VGH-VGL| ≦ 30			Volt	
Input voltage	Vin	-0.3	-	IOVCC+0.3	Volt	
HS input voltage	Vhsin	-0.3	-	2	Volt	
Operating Temperature	Topr	-20	-	+70	℃	
Storage Temperature	Tstg	-30	-	+80	℃	

6-1-2 Absolute Maximum Ratings (CTP)

Item	Symbol	Min	Typ	Max	Unit
System power supply voltage	VDD			3.6	V
High voltage power supply	V_{PVDD_CP}		3.6	3.7	V
Analog input voltage	V_{INANA}			VDD	V
Digital input voltage	V_{INDIG}			5	V
Storage temperature	T_{STG}	-40		150	℃

Notes: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

6-2 Operating Conditions

6-2-1 Operating Conditions (TFT) (Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply	VCC	-	2.6	3.0	3.6	Volt
	IOVCC	-	1.65	1.8	1.95	Volt
Level Input Voltage (Digital signal)	VIH	-	0.7* IOVCC	-	IOVCC	Volt
	VIL	-	GND	-	0.3* IOVCC	Volt
	VOH	-	0.8* IOVCC	-	IOVCC	Volt
	VOL	-	GND	-	0.2* IOVCC	Volt
Current for Driver	IDD	VCC=3.0V	-	TBD	-	mA

6-2-2 Operating Conditions (CTP)

Table 5-2: Power Supply

Item	Symbol	Min	Typ.	Max	Unit
System power supply voltage	VDD	2.8	3.3	3.6	V
Ambient operating temperature	T_A	-40		85	℃
Junction Temperature	T_J			125	℃

Table 5-3: DC Characteristics (T_{opr} = 25℃)

Item	Symbol	Min	Typ.	Max	Unit
Input Voltage, High 1	$(V_{IH1})^1$	1			V
Input Voltage, High 2	$(V_{IH2})^2$	1.3			V
Input Voltage, Low	(V_{IL})			0.5	V
Output Voltage, High 1	$(V_{OH})^3$		See Note3		V
Output Voltage, Low	(V_{OL})			0.1	V

Specifications are subjected to change without notice.

Notes:

1. **V_{IH1} includes pins CHIP_EN, SDA, SCL, INT**
2. **V_{IH2} includes pin EXT_CLK**
3. **V_{OH} is for INT output voltage level which is programmable by registers. Typical values are 1.2V/1.5V/1.8V/V_{VDD}.**

6-3 AC Characteristics

6-3-1 AC Characteristics (TFT)

6-3-1-1 MIPI AC Characteristics

6-3-1-1-1 High Speed Mode - Clock Timings

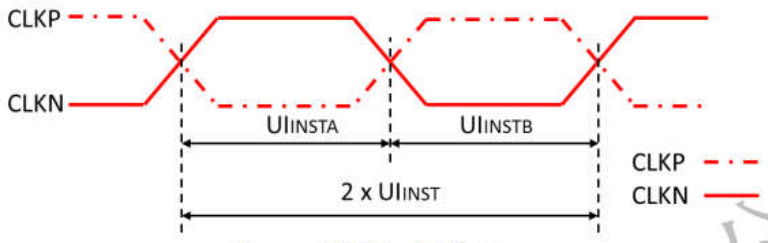


Figure 4-5 Clock Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CLK P/N	2xUIINST	Double UI instantaneous	2.5		12.5	ns	
CLK P/N	UIINSTA, UIINSTB	UI instantaneous Half	1.25		6.25	ns	1,2

***Note** 1*: UI = UIINSTA = UIINSTB.

***Note** 2*: ICNL9707 can support max 600Mbps/lane at 4 lane and max 800Mbps/lane at 3 lane application.

6-3-1-1-2 High Speed Mode - Clock / Data Timings

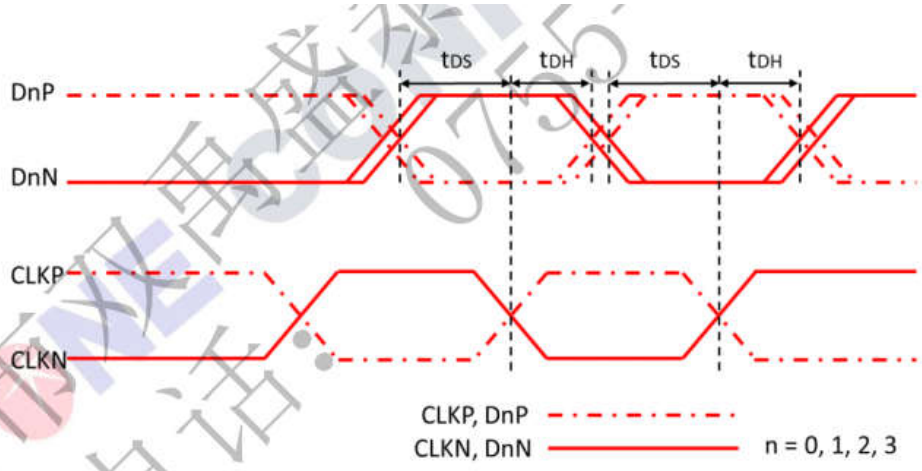


Figure 4-6 DSI Clock / Data Timings

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N (n=0,1,2 and 3)	tDS	Data to Clock Setup time	0.15*UI			UI	
	tDH	Clock to Data Hold time	0.15*UI			UI	

6-3-1-1-3 High Speed Mode - Rising and Falling Timings

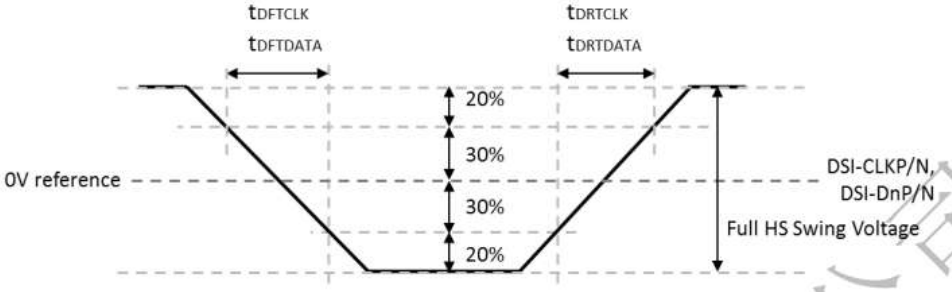


Figure 4-7 Rsing and Falling Timings

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Differential Rise Time for Clock	tDRTCLK	CLKP/N	150pS		0.3*UI		2,3
Differential Rise Time for Data	tDRTDATA	DnP/N	150pS		0.3*UI		1,2,3
Differential Fall Time for Clock	tDFTCLK	CLKP/N	150pS		0.3*UI		2,3
Differential Fall Time for Data	tDFTDATA	DnP/N	150pS		0.3*UI		1,2,3

***Note* 1:** DnP/N, n =0,1,2 and 3.
***Note* 2:** The display module has to meet timing requriements,which are defined for the transmitter (MCU) on MIPI D-PHY standard.
***Note* 3:** DSI-CLK+ = CLKP, DSI-CLK- =CLKN, DSI-D0+ =D0P, DSI-D0- =D0N.

6-3-1-1-4 Low Speed Mode - Bus Turn Around

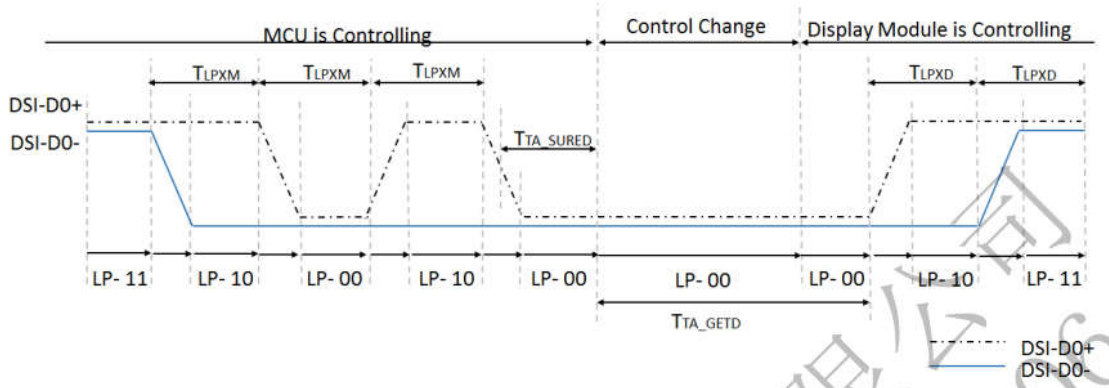


Figure 4-8 Bus Turnaround (BTA) from MCU to display module Timing

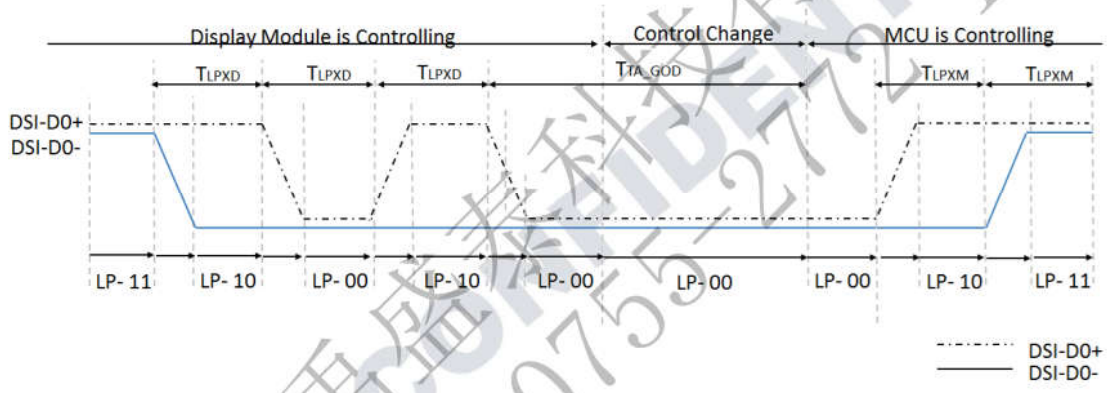


Figure 4-9 Bus Turnaround (BTA) from Display module to MCU Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	T_{LPXM}	Length of LP-00,LP-01,LP-10 or LP11 periods MCU to Display Module	50		75	nS	1
D0P/N	T_{LPXD}	Length of LP-00,LP-01,LP-10 or LP11 periods Display Module to MCU	50		75	nS	1
D0P/N	T_{TA_SURED}	Time-out before the Display Module starts driving	T_{LPXD}		2* T_{LPXD}	nS	1
D0P/N	T_{TA_GETD}	Time to drive LP-00 by Display Module	5* T_{LPXD}			nS	1
D0P/N	T_{TA_GOD}	Time to drive LP-00 after turnaround request -MCU	4 * T_{LPXD}			nS	1

Note 1: D0P = DSI-D0+, D0N = DSI-D0-.

6-3-1-1-5 Data Lanes from Low Power Mode to High Speed Mode

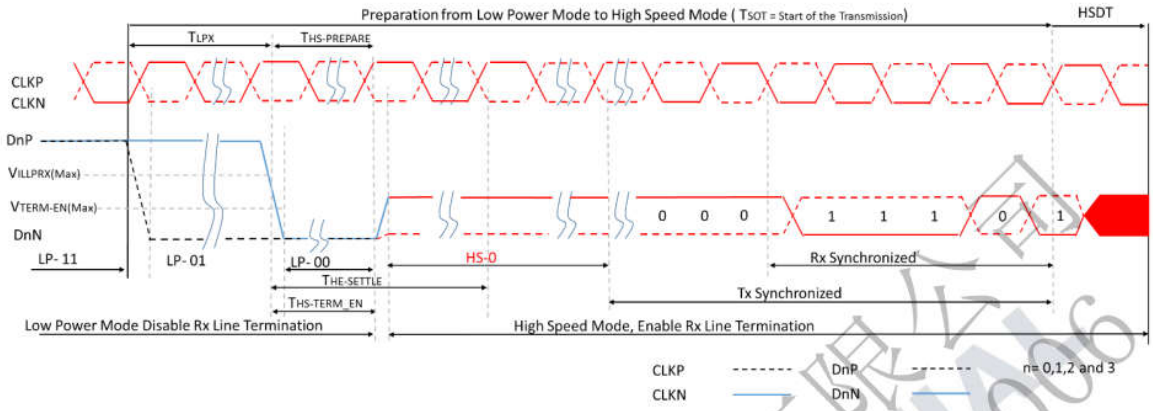
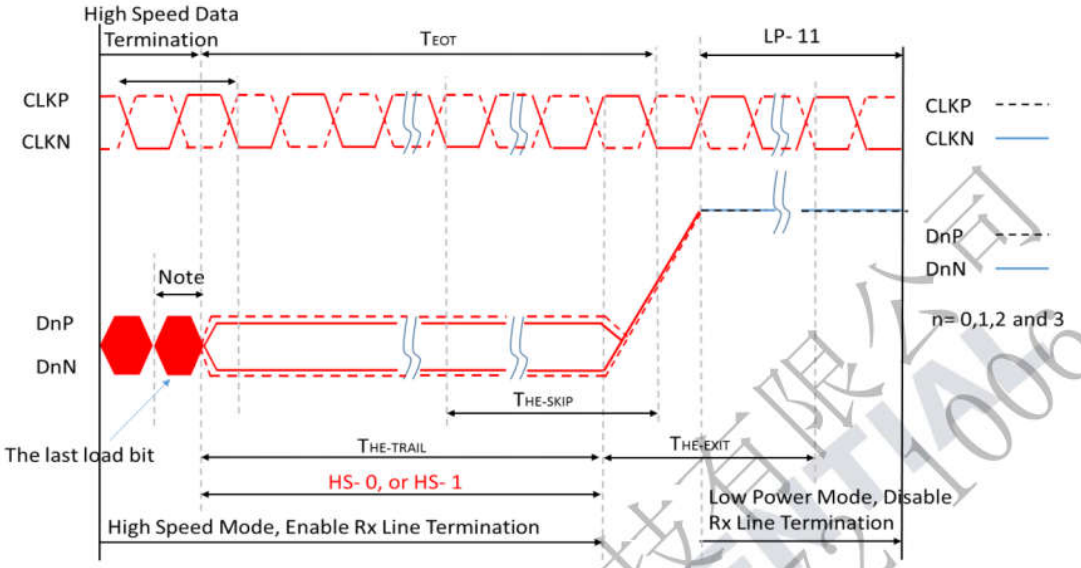


Figure 4-10 Data Lanes from Low Power Mode to High Speed Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	TLPX	Length of any Low Power State Period	50			nS	1
DnP/N	THS-PREPARE	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
DnP/N	THS-TREM-EN	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

Note 1: DnP/N, n=*0,1,2 and 3.*

6-3-1-1-6 Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Figure 4-11 Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	THS-SKIP	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
DnP/N	THS-EXIT	Time to drive LP-11 after HS burst	100			nS	1

Note 1: DnP/N, n=*0,1,2 and 3.*

6-3-1-1-7 DSI Clock Burst – High speed mode to /from Low Power Mode

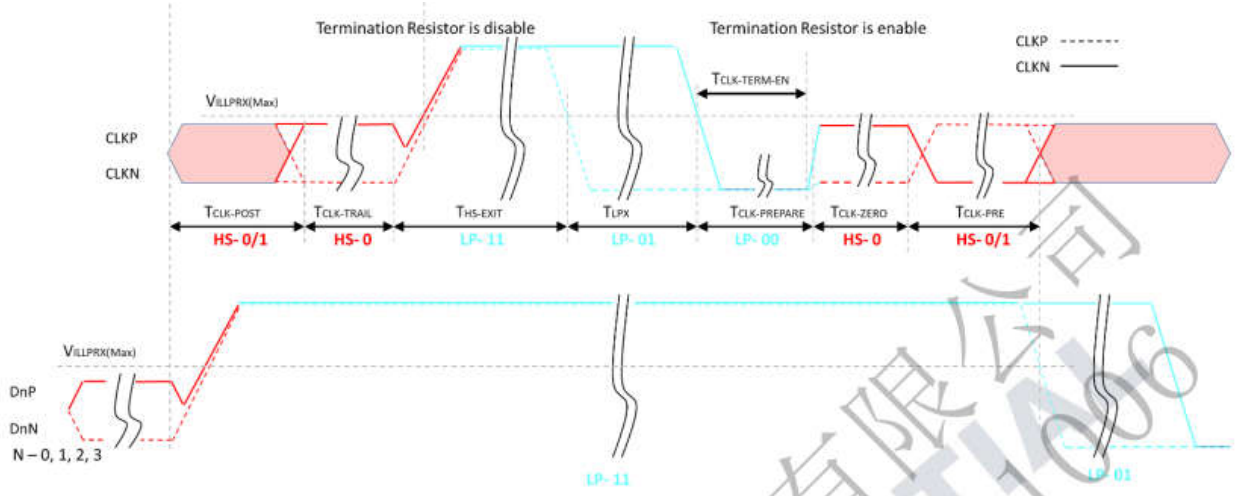


Figure 4-12 Clock Lane –High speed mode to / from Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CKP/N	TCK-POST	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52*UI			nS	
CKP/N	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CKP/N	THS-EXIT	Time to drive LP-11 after HS burst	100			nS	
CKP/N	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CKP/N	TCLK-TERM-EN	Time-out at Clock Lane to enable HS termination			38	nS	
CKP/N	TCLK-PREPARE+ TCLK-ZERO	Minimum lead HS-0 drive period before starting Clock	300			nS	
CKP/N	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			nS	

6-3-1-2 Reset Input Timing

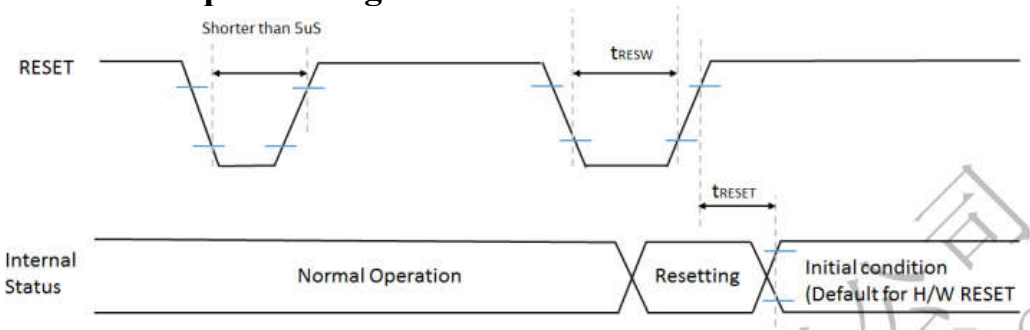


Figure 4-13 Reset Input Timing

Table 4-2 Reset Input Timing

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	tRESW	Reset "L" pulse width		10			uS	1
	tRESET	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	5

***Note* 1:** Condition : Ta =25℃.

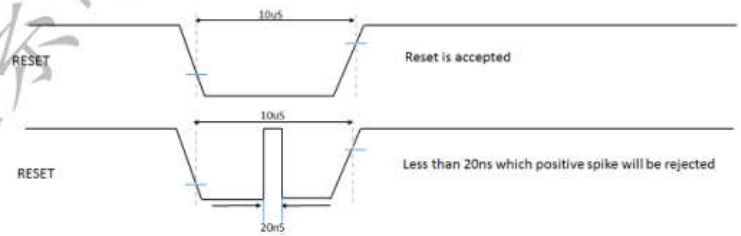
***Note* 2:** Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

RESET Pulse	Action
Less than 5us	Reset Rejected
More than 10uS	Reset
Between 5us and 10uS	Reset Start

***Note* 2:** During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

Note3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time (tRESET) within 5ms after a rising edge of RESET.

***Note 4*:** Spike Rejection also applies during a valid reset pulse as shown below:



***Note 5*:** It is necessary to wait 5ms after releasing RESET when sending commands, and Sleep Out command can not be sent within 120ms.

6-3-1-3 Power On/ OFF Sequence

6-3-1-3-1 Power ON Sequence

Applied Power: IOVCC, VCI

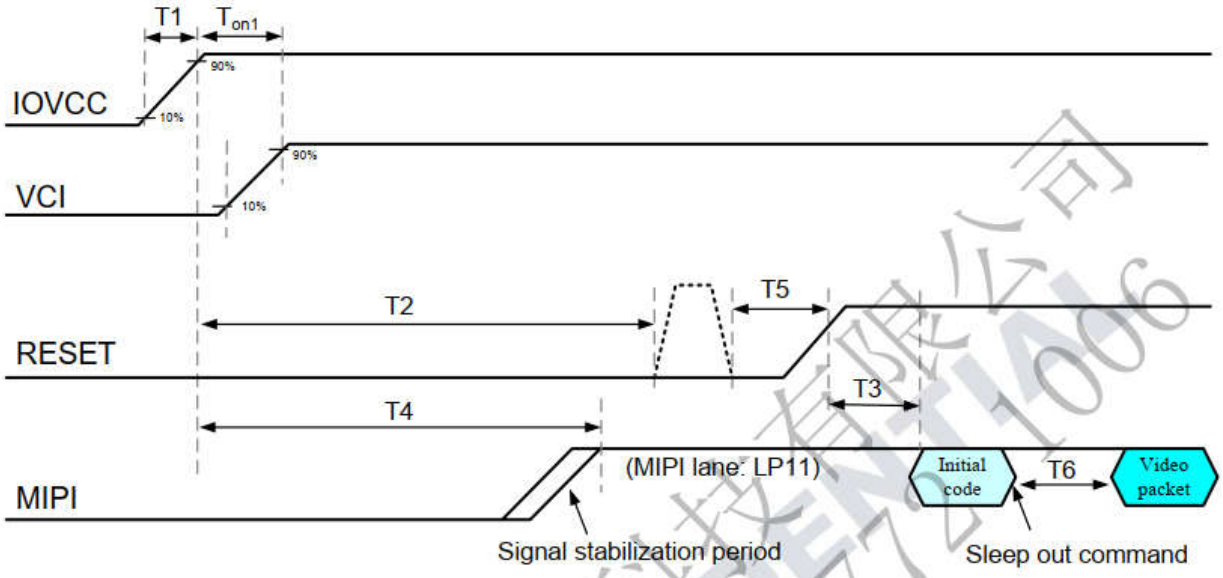


Figure 7-1 Power on sequence at PCCS[1:0]=[1,0] mode

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

6-3-1-3-2 Power OFF Sequence

Application Power: IOVCC, VCI,

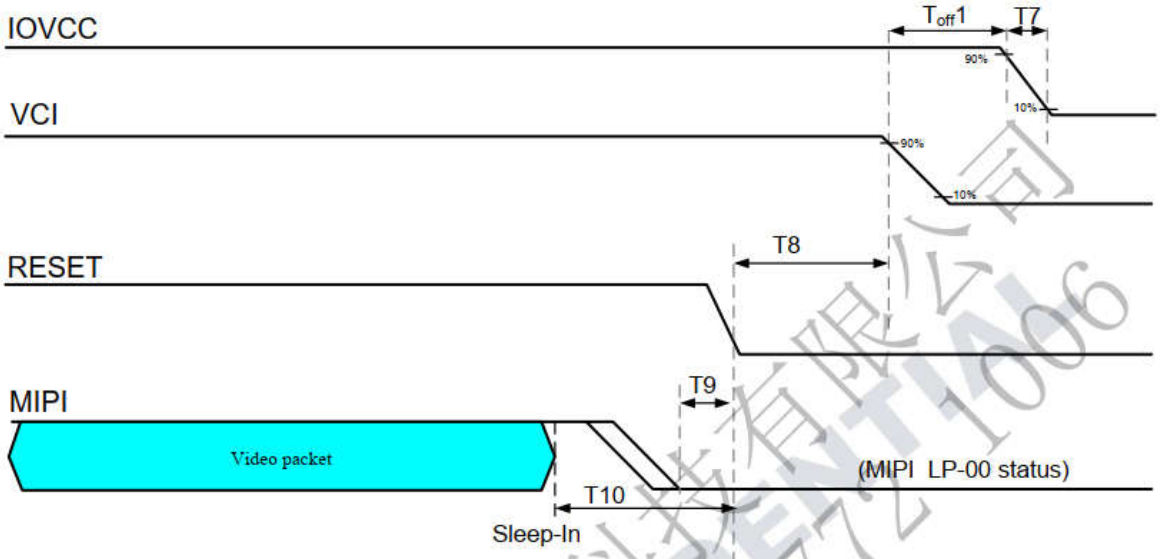


Figure 7-3 Power off sequence at PCCS[1:0]=[1,0] mode

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

6-3-2 AC Characteristics (CTP)

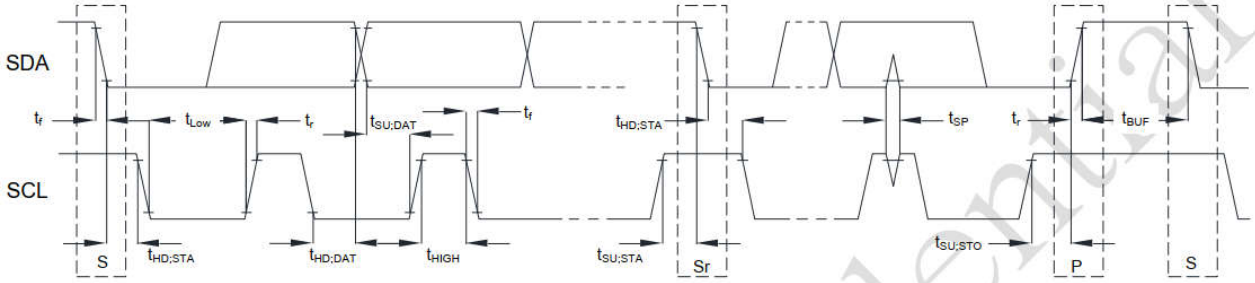


Figure 5-1: The timing of I^2C Interface

Table 5-5: Characteristics of the SDA and SCL bus lines

Symbol	Parameter	100KHz			400KHz		
		Min	Max	Unit	Min	Max	Unit
f_{SCL}	SCL clock frequency	0	100	kHz	0	400	KHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	μs	0.6	–	μs
t_{LOW}	LOW period of the SCL clock	4.7	–	μs	1.3	–	μs
t_{HIGH}	HIGH period of the SCL clock	4.0	–	μs	0.6	–	μs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	–	μs	0.6	–	μs
$t_{HD;DAT}$	Data hold time	0	3.45	μs	0	0.9	μs
$t_{SU;DAT}$	Data set-up time	250	–	ns	100	–	ns
t_r	Rise time of both SDA and SCL signals	–	1000	ns	–	300	ns
t_f	Fall time of both SDA and SCL signals	–	300	ns	–	300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0	–	μs	0.6	–	μs
t_{BUF}	Bus free time between a STOP and START condition	4.7	–	μs	1.3	–	μs

7. Optical Characteristics

Item		Symbol	Conditions	Specifications			Unit	Note
				Min	Typ	Max		
Transmittance		T(%)	-	3.74	4.4	-	-	-
Contrast Ratio		CR	θ=0 Normal Viewing angle	1000	1500	-		(1) (2)
Response time		TR+TF	-	-	25	35	ms	(1) (3)
NTSC			-	65	70	-	%	
Viewing angle	Hor.	Θx+	CR≧10	75	85	-	deg.	-
		Θx-		75	85	-		
	Ver.	Θy+		75	85	-		
		Θy-		75	85	-		

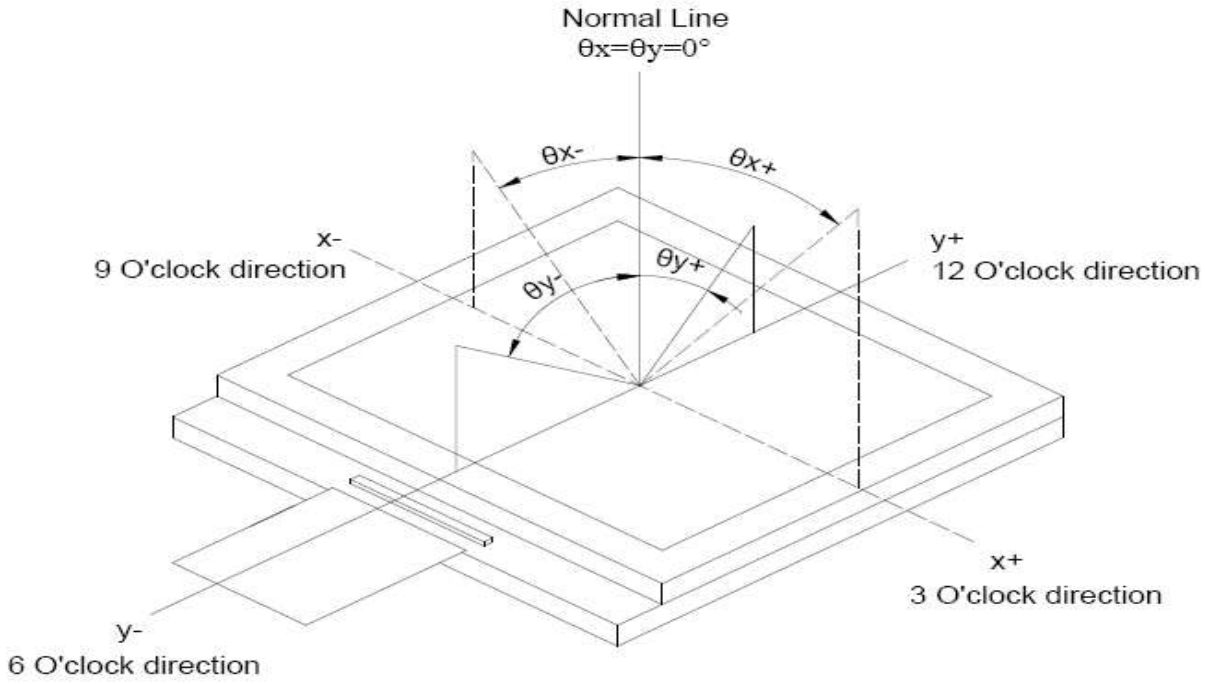
Measuring Condition

1. Measuring surrounding: dark room
2. Ambient temperature: 25±2℃
3. 30 min. Warm-up time.

Color of CIE Coordinate:

Item		Symbol	Condition	Min.	Typ.	Max.
Chromaticity Coordinates (Transmissive)	Red	x	θ = φ = 0° LED Backlight Color Degree	TBD	0.656	TBD
		y		TBD	0.318	TBD
	Green	x		TBD	0.255	TBD
		y		TBD	0.576	TBD
	Blue	x		TBD	0.137	TBD
		y		TBD	0.098	TBD
	White	x		TBD	0.293	TBD
		y		TBD	0.322	TBD

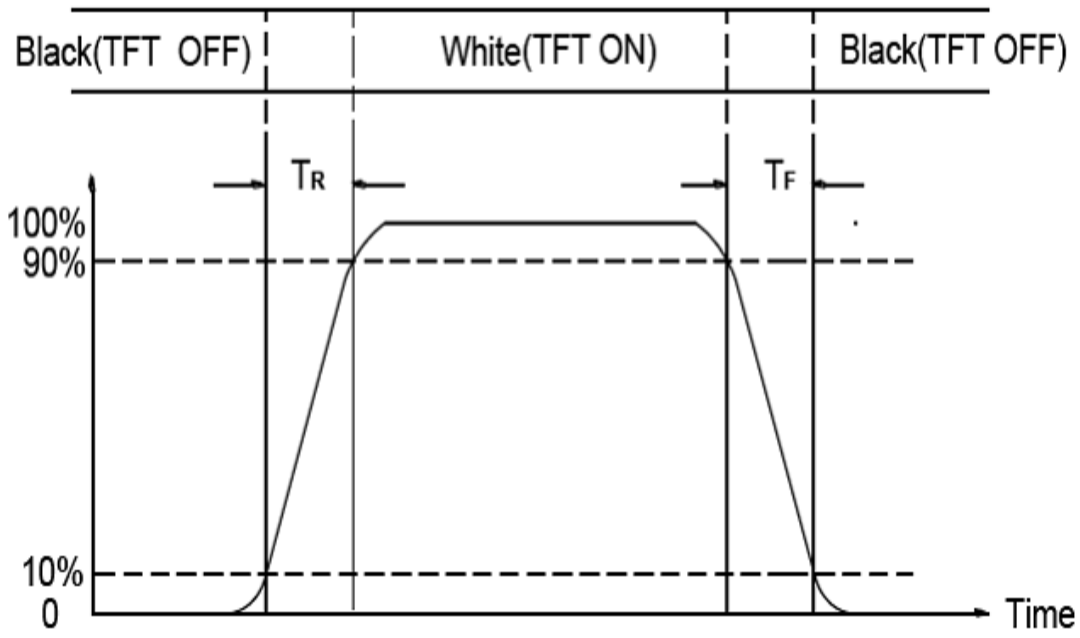
Note (1) Definition of Viewing Angle :



Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black}}$$

Note (3) Definition of Response Time : Sum of TR and TF



8. Interface Pin Assignment

8-1 LCM FPC Interface

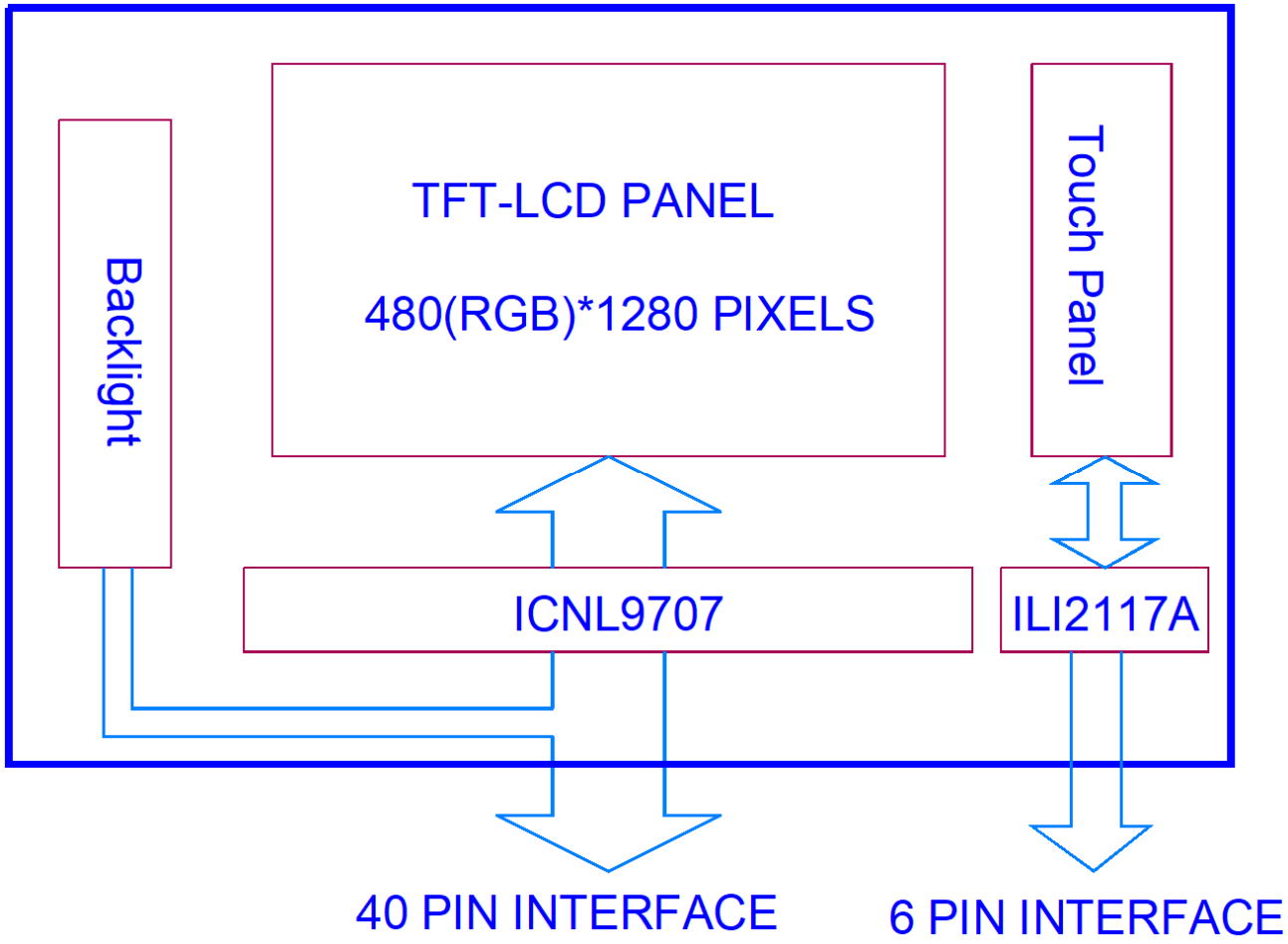
No.	Symbol	Function
1	GND	Power ground
2	D0P	MIPI-DSI Data differential signal input pins.
3	D0N	MIPI-DSI Data differential signal input pins.
4	GND	Power ground
5	D1P	MIPI-DSI Data differential signal input pins.
6	D1N	MIPI-DSI Data differential signal input pins.
7	GND	Power ground
8	CP	MIPI-DSI Clock differential signal input pins.
9	CN	MIPI-DSI Clock differential signal input pins.
10	GND	Power ground
11	D2P	MIPI-DSI Data differential signal input pins.
12	D2N	MIPI-DSI Data differential signal input pins.
13	GND	Power ground
14	D3P	MIPI-DSI Data differential signal input pins.
15	D3N	MIPI-DSI Data differential signal input pins.
16	GND	Power ground
17	GND	Power ground
18	IOVCC	Power supply for the logic power and I/O circuit.
19	IOVCC	Power supply for the logic power and I/O circuit.
20	NC	Not connect
21	NC	Not connect
22	NC	Not connect
23	GND	Power ground
24	RESET	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
25	VSP	Not connect
26	VSN	Not connect
27	GND	Power ground
28	LEDK	Power supply Cathode input for backlight.
29	LEDK	Power supply Cathode input for backlight.
30	GND	Power ground

31	NC	Not connect
32	GND	Power ground
33	GND	Power ground
34	NC	Not connect
35	LEDA	Power supply Anode input for backlight.
36	LEDA	Power supply Anode input for backlight.
37	GND	Power ground
38	VCI	Power supply to the analog circuit.
39	VCI	Power supply to the analog circuit.
40	TE	Tearing Effect pin.

8-2 CTP FPC Interface

No.	Symbol	Function	Remark
1	INT	Touch panel interrupt output	
2	SDA	Touch panel I2C data	
3	SCL	Touch panel I2C clock	
4	RESET	Touch panel reset	
5	VDD	Touch panel power supply	
6	GND	Touch panel Ground	

9. Block Diagram



10. Backlight

1. Standard Lamp Styles (Edge Lighting Type):
The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption:

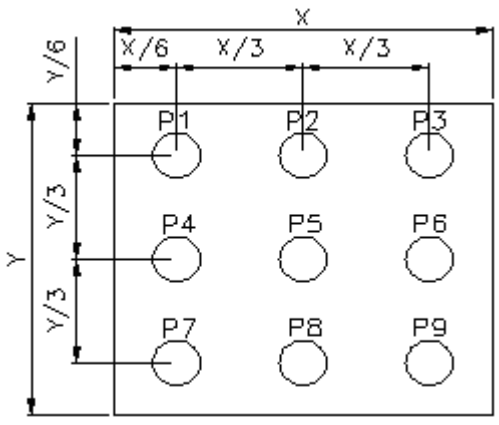
2. The Main Advantages of the LED Backlight are as following:
2.1 The brightness of the backlight can simply be adjusted.
By a resistor or a potentiometer.

3. Data About LED Backlight: (Ta=25°)

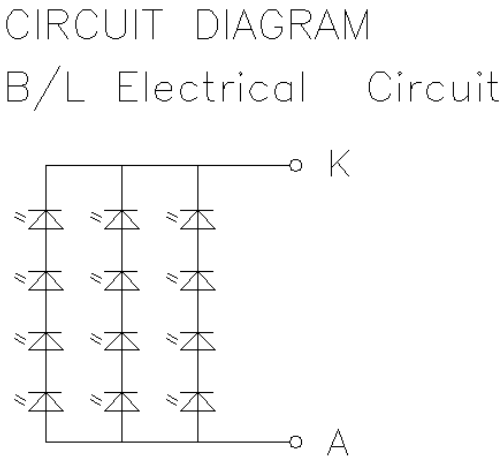
PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
Supply Current	I	-	120	-	mA	-	
Supply Voltage	V	10.8	12.4	14.0	V	If=120mA	1
Luminous Intensity for LCM+CTP	IV	250	340	-	Cd/m2		2
Uniformity for LCM+CTP	-	70	-	-	%		3
Life Time	-	20000	-	-	Hr.		4
Color	White						

NOTE:
1. Backlight Only
2. Average Luminous Intensity of P1-P9
3. Uniformity = Min/Max * 100%
4. LED life time defined as follow: the final brightness is at 50% of original brightness

Measured Method: (X*Y: Light Area)



Internal Circuit Diagram



Using aperture of 1°, distance 50cm.

11. Standard Specification for Reliability

11–1. Standard Specifications for Reliability

No	Item	Description
01	High temperature operation	The sample should be allowed to stand at 70℃ for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
02	Low temperature operation	The sample should be allowed to stand at -20℃ for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
03	High temperature storage	The sample should be allowed to stand at 80℃ for 240 hours under no-load condition, and then returning it to normal temperature condition, and allowing it stand for 2 hours.
04	Low temperature storage	The sample should be allowed to stand at -30℃ for 240 hours under no-load condition, then returning it to normal temperature condition, and allowing it stand for 2 hours.
05	Moisture storage	The sample should be allowed to stand at 60℃,90%RH MAX for 240 hours under no-load condition, then taking it out and drying it at normal temperature for 2 hours.
06	Thermal shock storage	The sample should be allowed to stand the following 10 cycles : -30℃ for 30 minutes → normal temperature for 5 minutes → +80℃ for 30 minutes → normal temperature for 5 minutes, as one cycle.
07	Packing vibration	Frequency range : 10Hz ~ 55Hz Amplitude of vibration : 1.5mm Sweep time: 12 min X,Y,Z 2 hours for each direction.
08	Packing drop test	According to ISTA 1A 2001.
09	Electrical Static Discharge	Air: ±6KV 150pF/330Ω 5 times
		Contact: ±4KV 150pF/330Ω 5 time

*Sample size for each test item is 3~5pcs

11 - 2. Testing Conditions and Inspection Criteria

For the final test the testing sample must be stored at room temperature for 24 hours, after the tests listed in Table 11-1, Standard specifications for Reliability have been executed in order to ensure stability.

No	Item	Test Model	In section Criteria
01	Current Consumption	Refer To Specification	The current consumption should conform to the product specification.
02	Contrast	Refer To Specification	After the tests have been executed, the contrast must be larger than half of its initial value prior to the tests.
03	Appearance	Visual inspection	Defect free.

11- 3. MTBF

MTBF	Functions, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (25±5℃), normal humidity (50±10% RH), and in area not exposed to direct sun light.

12. Specification of Quality Assurance

12-1. Purpose

This standard for Quality Assurance should affirm the quality of LCD module products to supply to purchaser by YEEBO CORPORATION (Supplier).

12-2. Standard for Quality Test

a. Inspection:

Before delivering, the supplier should take the following tests, and affirm the quality of product.

b. Electro-Optical Characteristics:

According to the individual specification to test the product.

c. Test of Appearance Characteristics:

According to the individual specification to test the product.

d. Test of Reliability Characteristics:

According to the definition of reliability on the specification for testing products.

e. Delivery Test:

Before delivering, the supplier should take the delivery test.

(i) Test method: According to **ISO2859-1.**General Inspection Level Ⅱ take a single time.

(ii) The defects classify of AQL as following:

Major defect: AQL = 0.65

Minor defect: AQL = 2.5

Total defects: AQL = 2.5

12-3. Non- conforming Analysis & Deal With Manners

a. Non- conforming Analysis:

(i) Purchaser should supply the detail data of non- conforming sample and the non-conforming.

(ii) After accepting the detail data from purchaser, the analysis of non- conforming should be finished in two weeks.

(iii) If supplier can not finish analysis on time, must announce purchaser before 3 days.

b. Disposition of non- conforming:

(i) If find any product defect of supplier during assembly time, supplier must change the good product for every defect after recognition.

(ii) Both supplier and customer should analyze the reason and discuss the disposition of non- conforming when the reason of nonconforming is not sure.

12-4. Agreement items

Both sides should discuss together when the following problems happen.

a. There is any problem of standard of quality assurance, and both sides should think that must be modified.

b. There is any argument item which does not record in the standard of quality assurance.

c. Any other special problem.

12-5. Standard of The Product Appearance Test

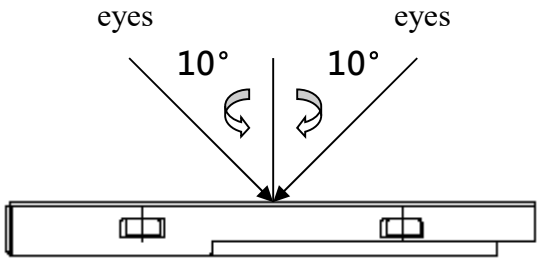
a. Manner of appearance test:

(i) The test must be under 20W × 2 or 40W fluorescent light, and the distance of view must be at 30±5cm.

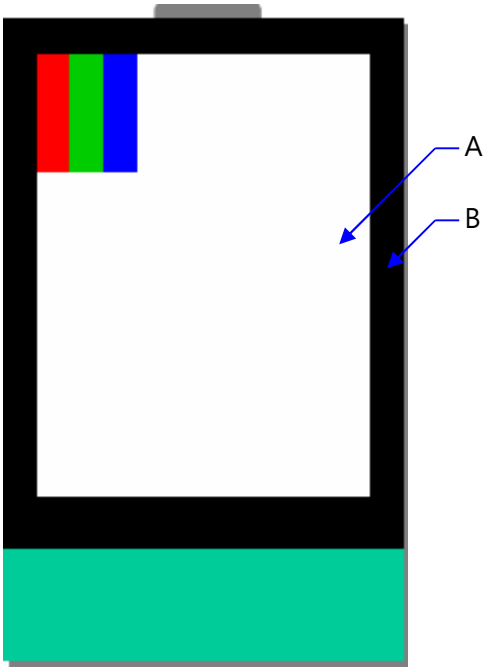
(ii) When test the model of transmissive product must add the reflective plate.

(iii)The test direction is base on around 10° of vertical line.

(iiii)Temperature: 25±5℃ Humidity: 60±10%RH



(iv) Definition of area:



A. Area: Viewing area.

B. Area: Out of viewing area.
(Outside viewing area)

b. Basic principle:

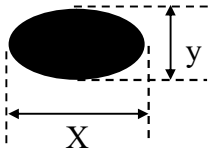
(i) It will accord to the AQL when the standard can not be described.

(ii) The sample of the lowest acceptable quality level must be discussed by both supplier and customer when any dispute happened.

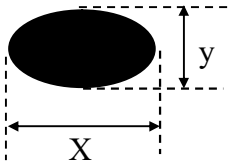
(iii) Must add new item on time when it is necessary.

c. Standard of inspection: (Unit: mm)

12-6. Inspection specification
Defect out of viewing area can be neglected.

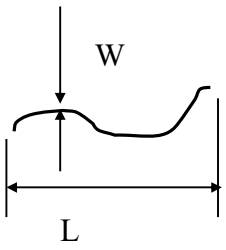
<table>
<tr><th>Item</th><th>Specification Unit : mm</th><th>AQL</th></tr>
<tr><td>Electrical Testing</td><td>1.1 Open
1.2 Short
1.3 T/P failure
1.4 Missing vertical, horizontal segment, segment contrast defect.
1.5 Missing character, dot or icon.
1.6 Display malfunction.
1.7 No function or no display.
1.8 Current consumption exceeds product specifications.
1.9 LCD viewing angle defect.
1.10 Mixed product types.
1.11 Flicker</td><td>0.65</td></tr>
<tr><td>explosion-proof film bubble/Concave and convex point/indentation / Contamination</td><td>
<table>
<tr><th>D</th><th>Acceptable numbers</th></tr>
<tr><td>≤0.25</td><td>ignored (No more than five spots within 5mm)</td></tr>
<tr><td>0.25＜D≤0.5</td><td>3</td></tr>
<tr><td>0.5＜D≤0.8</td><td>2</td></tr>
<tr><td>0.8＜D≤1.5</td><td>1</td></tr>
<tr><td>D＞1.5</td><td>NG</td></tr>
</table>


D=(x+y)/2
1. Product’s front side checked according to this specification, back side ignored, but light leakage is not allowed.
2. Printing ink peel off is not allowed.
3. The particle will be ignored when it is removable by cleaning

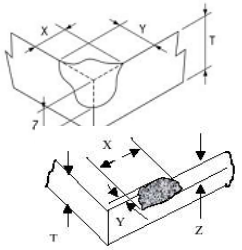
* Densely spaced: No more than two spots within 10mm</td><td>2.5</td></tr>
<tr><td>Black spots / White spots /Bright spots/ Color spots /polluted inside/ punctured</td><td>
<table>
<tr><th>D</th><th>Acceptable numbers</th></tr>
<tr><td>≤0.15</td><td>ignored (No more than five spots within 5mm)</td></tr>
<tr><td>0.15＜D≤0.3</td><td>3</td></tr>
<tr><td>0.3＜D≤0.5</td><td>2</td></tr>
<tr><td>D＞0.5</td><td>NG</td></tr>
</table>


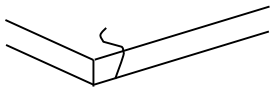
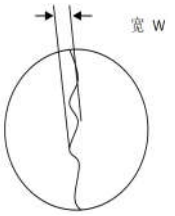
D=(x+y)/2
1. Product’s front side checked according to this specification, back side ignored, but light leakage is not allowed.
2. Printing ink peel off is not allowed.
3. The particle will be ignored when it is removable by cleaning

* Densely spaced: No more than two spots within 10mm</td><td>2.5</td></tr>
</table>

<table>
<tr>
<td>Linear Object: Fiber, scurf, scratches and other linear defects (not affecting function)</td>
<td>
<table>
<tr><th>W</th><th>L</th><th>Acceptable numbers</th></tr>
<tr><td>≤0.05</td><td>≤6</td><td>ignored (No more than five lines within 5mm)</td></tr>
<tr><td>0.05＜W≤0.25</td><td>≤6</td><td>2</td></tr>
<tr><td>W〉0.25</td><td></td><td>NG</td></tr>
</table>


The reverse side scratches, not affect to the electronic circuit, cannot find the scratches from the front side is acceptable

* Densely spaced: No more than two lines within 10mm
</td>
<td>2.5</td>
</tr>
<tr>
<td>Glass edge chipping、edge breakage</td>
<td>
<table>
<tr><td colspan="2">Edge breakage can’t affect visual effection (edge breakage can’t cause damage to circuit); over lens have no visual damage</td></tr>
<tr><td>conditions</td><td>Acceptable numbers</td></tr>
<tr><td>X≤1.5mm,Y≤2mm,Z≤T</td><td>4</td></tr>
</table>


</td>
<td>2.5</td>
</tr>
<tr>
<td>Glass broken</td>
<td>Visual broken is NG, and there is no potential fault.
  </td>
<td>0.65</td>
</tr>
<tr>
<td>1. V/A printed edges sawtooth inspected according to this standard
2. LOGO’s sawtooth</td>
<td>
<table>
<tr><td colspan="2">Some contentious defect judged according to samples</td></tr>
<tr><td>Product type</td><td>Conditions</td></tr>
<tr><td>Same size</td><td>1、width below 0.2 inch（included）ignored，above 0.2 NG
2、Length not accounted</td></tr>
</table>


</td>
<td>2.5</td>
</tr>
<tr>
<td>Specific dimension</td>
<td>In accordance with product outline drawing or specification (key dimension) or engineering sample.</td>
<td>2.5</td>
</tr>
<tr>
<td>Glue overflow/Frame</td>
<td>1. Glue overflow exceed 0.2mm to the black frame is not allowed.
  </td>
<td>2.5</td>
</tr>
</table>

FPC	Bonding bubble/ Misalignment	FPC golden finger hot pressure's bubble or impurity diameter shall be below 1/2 of the pressed area, pressed deviation shall not exceed 1/2 of the silver line width, and 40X microscope cannot have obvious cracks.	0.65
	Folded mark （minor fault）	Linearity irreversibility folded mark and acute angle folded mark is NG.	2.5
	EMI FILM （minor fault）	Surface broken, scratched≦0.3mm Surface broken below 5mm can be modified by print ink, after modified, the result shall be achieved to EMI	2.5

13. Handling Precaution

13.1 Warranty

This product has been manufactured to specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we will not take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

1. We cannot accept responsibility for any defect arise after additional process of the product (including disassembly and reassembly), after product delivery.
2. We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
3. We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.
4. We cannot accept responsibility for industrial property, which may arise through the use of your product, with exception to those issues relating directly to the structure or method of manufacturing of our product 3months from YEEBO production.
5. The liability of YB is limited to repair or replacement on the terms set forth below. YB will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between YB and the customer, YB will only replace or repair any of its CTP which is found defective electrically or visually when inspected in accordance with YB GENERAL CTP INSPECTION STANDARD.

13.2. Precautions in Use of CTP Module

13.2-1. Handling of CTP Module

13.2-1-1 Please operate the capacitive touch panel by touch the panel surface with finger or electric pen

13.2-1-2 Store the products at the temperature and humidity mentioned in the specification in a good package do not expose the products under direct sunlight.

13.2-1-3 Do not hit the capacitive touch panel in strong force , or drop it down, it is made of glass and friable.

13.2-1-4 Put on finger coats · glovers or mask to protect the products from fingerprint of stain. Do not upload/unload the touch panel by holding the FPC cable. Do not bend the FPC cableoften or pull it hard when installing, as FPC cable is soft and connected to touch panel body.

13.2-1-5 Pay attention to the prevention from high voltage and static electricity.

13.2-2 Storage

13.2-2-1 Store in ambient temperature of 25±10℃, and relative humidity of 50±10%RH. Do not expose to sunlight or fluorescent light.

13.2-2-2 Storage in a clean environment, free from dust, active gas, and solvent.

13.2-2-3 Store in anti-static electricity container.

13.2-2-4 Store without any physical load.

13.2-2-5 Appearance,3months;Function,1year;within the validity, failed CTP can be replaced 1 to 1

13.3 Guarantee

Our products meet requirements of the environment.YEEBO ROHS requirement is based on European Union Directive 2011/65/EU (ROHS) Requirements and Update.